SCRAMNet+ Network

ISA
Hardware Reference

Document No. D-T-MR-ISA#####-A-0-A5

FOREWORD

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FCC

This product is intended for use in industrial, laboratory or military environments. This product uses and emits electromagnetic radiation which may interfere with other radio and communication devices. The user may be in violation of FCC regulations if this device is used in other than the intended market environments.

CE

Please note: As a component part of another system, this product has no intrinsic function and is therefore not subject to the European Union CE EMC directive 89/336/EEC.

TABLE OF CONTENTS

HOW TO USE THIS MANUAL

APPENDICES

FIGURES

TABLES

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1.HOW TO USE THIS MANUAL

1.1 Scope

This document is a reference manual for the **SCRAMNet+** ISA host interface board.

This document provides a physical and functional description of the **SCRAMNet+** ISA board designed for ISA bus host system.

This information is intended for systems designers, engineers and network installation personnel.

The reader should have at least a systems level understanding of general computer processing, memory and hardware operation and a systems level understanding of the specific host processor.

1.2 Organization

This document is divided into six sections: Introduction, Description, Installation, Operation, Control/Status Register Description, and Physical Features.

1.0 Introduction:	An overview of the **SCRAMNet+** ISA product and host interface compatibility.
2.0 Description:	A functional description of the **SCRAMNet+** network node.
3.0 Installation:	Procedures for unpacking, configuring and installing the **SCRAMNet+** ISA node board.
4.0 Operation:	A discussion of how the node works; including Control/Status registers, Shared Memory, Message Passing, Data Filtering, Interrupt Initialization and Handling, Auxiliary Control RAM, and other features.
5.0 CSR Description:	A detailed explanation of all the Control/Status Registers.
6.0 Physical Features:	A description of the physical features of the **SCRAMNet+** ISA board.

1.3 Appendices

A - CSR Summary:	A quick reference summary of the Control/Status Registers by bit, function and name.
B - ISA CSR Summary:	A reference summary of the ISA Control/Status Registers by bit and function.
C - Specification Summary:	General board specifications, Bus Voltage Specification, part number breakdown, and Fiber Optic Bypass Switch specifications.
D - Configuration Aids:	Control/Status Register (CSR) Reference Sheet and network configuration form.
E - ISA Configuration	

Manager:	A utility that simplifies configuration of default resource assignments for a **SCRAMNet** card.
F - Glossary:	A glossary of words, phrases and terms used in the reference manual.

1.4 Related Documentation

- *SCRAMNet Network Media User's Guide* (D-T-MU-MEDIA)—A description of network cabling hardware assessories for the **SCRAMNet+** Network.
- *SCRAMNet Network Programmer's Reference Guide* (C-T-MR-PROGREF)—This manual describes the basic operations of the **SCRAMNet** Network Interface Library routines for all of the supported host platforms using the **SCRAMNet** Network hardware. This manual is a guide to understanding the library routines and how they relate to the **SCRAMNet** Network control/status registers.
- *SCRAMNet Network Software Installation Manual for ISA Using DOS* (C-T-MI-MDXXIC)
- *SCRAMNet Network Windows DLL Reference Guide* (C-T-ML-WINDLL)—This manual defines a set of user routines that are exported by the Windows Dynamic Link Library(DLL) to aid in application development.
- *SCRAMNet Network Windows NT DLL Reference Guide* (C-T-ML-NTDLL)—This manual defines a set of user routines that are exported by the Windows NT DLL to aid in application development.
- *SCRAMNet Network Utilities Manual (C-T-MU-UTIL)*—This manual describes the use of SYSTRAN hardware, diagnostic software, **SCRAMNet+** EEPROM initialization software, and the **SCRAMNet** Monitor software.

2.0 INTRODUCTION

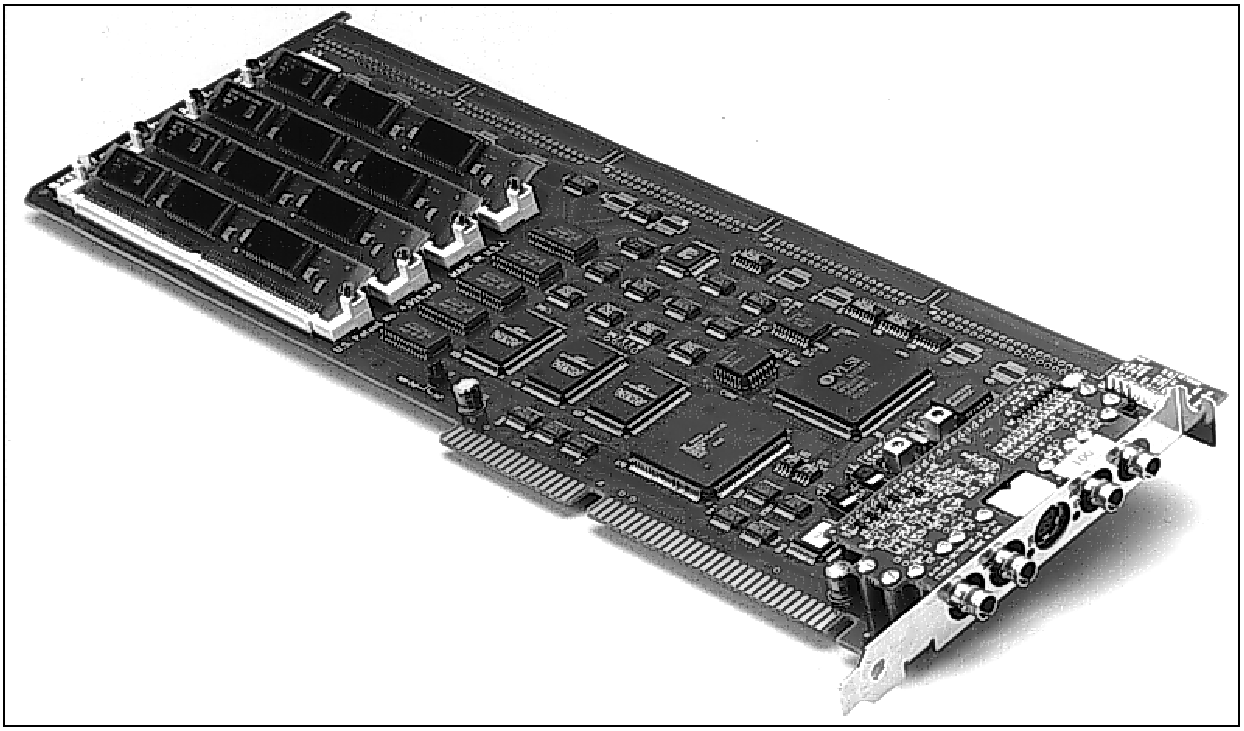

Figure 2-1 ISA Board

2.1 Overview

SCRAMNet+ (Shared Common Random Access Memory Network) is a communications network geared toward real-time applications, and based on a replicated, shared-memory concept.

The **SCRAMNet+** interface node board is backwards-compatible with the original **SCRAMNet** Classic product with the exception of the GOLD Ring communication protocol.

The **SCRAMNet+** ISA board requires a single slot in the computer chassis.

The **SCRAMNet+** board base address for Control/Status Registers is software configurable, and can be mapped to the I/O bus or memory bus. The 4 KB or 128 KB on-board shared memory can be upgraded to 512 KB, 1 MB, 2 MB, 4 MB or 8 MB random access memory (RAM). Installing any memory upgrade overrides the on-board shared memory.

2.2 Network Features

- A ring topology with 150 Mbit/s line transmission rate.
- A "Data Filter" that allows only data stored in shared memory that has changed to be passed to the network for communications to the other nodes.
- Field Upgrade Memory Options up to 8 MB of replicated, shared memory for each node processor.
- **SCRAMNet+** BURST Mode protocol (error correction disabled) with fixed-length-message packets of 82 bits.
- **SCRAMNet+** BURST PLUS Mode communication based on variable-length message packet to a maximum of either 256 bytes or 1024 bytes.
- **SCRAMNet+** PLATINUM Mode protocol (error correction enabled) with fixed-length-message packets of 82 bits.
- **SCRAMNet+** PLATINUM PLUS Mode communication based on variable-length message packet to a maximum of either 256 bytes or 1024 bytes.
- 256-node capacity on each ring.
- No operating or system software required to support network protocol.
- No network-dependent application software required.

2.3 Options

- Optional paired fiber-optic or coaxial transmission media
- Fiber Optic Bypass Switch for ring continuity when node power is off.
- Quad Switch—A switching control device that controls up to four nodes or sub-rings, eliminates the need for a separate Fiber Optic Bypass Switch, and functions as a repeater.

2.4 ISA Board Features

- Software configuration.
- Host virtual paging of any **SCRAMNet** memory size.
- Custom SIMM memory upgrade option.
- General-purpose counter.
- Error-interrupt mask.
- Dynamic shared-memory addressing.
- Network virtual paging for shared memory (CSR selectable).
- Variable-length message packet capability.
- Dual-port memory.
- Dual memory and error interrupt.
- Single-slot solution.
- 16/8 bit device selectable (software selectable)
- All memory sizes are scaleable to 8 KB, 16 KB, 32 KB, or 64 KB.

2.5 ISA Specification Level

The **SCRAMNet+** ISA board was designed in accordance with the ISA specification Version 3.11.

2.6 Hardware

- 16-bit ISA compliant.
- Maximum speed 8.33 MHz
- Supports bus level interrupts IRQ 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15.
- Less than 1.5 amps @ 5 volts only.
- Single-slot connection.

NOTE: The **SCRAMNet+** ISA board is a physical-memory device accessed via the ISA bus. The ISA bus has 24 address bits for memory. This limits the bus to 16 MB of addressable memory. If the host system has 16 MB of RAM installed, the ISA bus memory address space is consumed by the system RAM. This leaves no available address space for a physical-memory device on the ISA bus.

One solution is to reduce the amount of RAM in the host system. Ensure the reduction is sufficient to provide an “empty” space between the end of system RAM and the beginning of **SCRAMNet+** memory. Additionally, ensure **SCRAMNet+** memory is on an address boundary that matches the memory size of the **SCRAMNet+** board.

A second solution is to use the ISA card in memory-paging mode. This is accomplished by using the Configuration Manager. The Configuration Manager allows access to **SCRAMNet**+ shared memory below the one-megabyte boundary in page sizes ranging from 8 to 64 KB. See Appendix E for more information.

If reducing the system RAM size is not desirable, an alternative solution is to change the host system from an ISA-based system to an EISA-based system. The 32-bit bus allows up to 4 GB of address space. A **SCRAMNet+** EISA board can easily be mapped above any system RAM in the EISA bus address space.

2.7 PC Software

The objective of the software effort for the PC-Clone platforms, is to provide one software package that is adaptable to all of the environment combinations described below:

- ISA Bus
  SCRAMNet Classic/SCRAMNet-LX/SCRAMNet+
  16 bit Address Bus, 16 MB Max Address
- EISA Bus
  SCRAMNet Classic/SCRAMNet-LX/SCRAMNet+
  32 bit Address Bus, 4 GB Max Address

Since the **SCRAMNet** hardware is only accessible beyond the 1 MB boundary in a PC, this requires a DOS-Extender in addition to the compiler. A DOS-Extender is a package that allows an application program to put the 386/486 CPU into Protected Mode, which allows access to the address space beyond 1 MB. The current compiler supporting the **SCRAMNet** software is the Intel Code Builder Kit, which incorporates a Compiler and a DOS-Extender in one package.

The **SCRAMNet+** Diagnostic software executable is 386/486 compatible.
It requires 2 MB of system memory (excluding **SCRAMNet+** memory), and

runs under MS-DOS 3.3 and above and all 386 DPMI level .9 compliant host memory managers including the 386 enhanced mode of Microsoft Windows 3.1.

Shared memory exists anywhere above 640 KB in the PC host. Above 1 MB it is compatible as EXTENDED Memory and must be accessed via Protected Mode.

2.7.1 Configuration Options

The **SCRAMNet+** ISA board is configured by software. The configuration software locates the board using "Plug and Play" techniques. Full implementation of the PnP feature is not available because there is currently no method of identifying all non-PnP (Legacy) boards in the system. On PnP systems, the Basic Input/Output System (BIOS) or Operating System examines each device in order to allocate resource requirements. Since Legacy boards cannot be identified, a conflict in resource allocation is almost inevitable. Consequently, all boards are issued with a null resource requirement which will force the PnP system to leave the board inactive.

Legacy systems have no ability to assign resources. Consequently, the board must be manually configured using the **SCRAMNet+** configuration software. The **SCRAMNet+** configuration software allows interactive modification of the device's resource configuration. Once all of the desired changes have been made, the new default power-on configuration is written to the PnP EEPROM. The board is activated automatically following configuration. It can also be manually activated when necessary. The configuration software assigns resources only for **SCRAMNet+** on Legacy systems.

2.7.2 Host Virtual Paging

The **SCRAMNet+** ISA board offers the capability to page any **SCRAMNet+** memory size into 64 KB, 32 KB, 16 KB, or 8 KB. This is accomplished through the use of ISA registers CSR6 and CSR14. This is described in more detail in Section 3.0 INSTALLATION.

2.7.3 Compatibility

SCRAMNet+ Diagnostic source code and the Software Library are compatible with the following:

- Intel Code Builder Support
    - allows access up to 4 GB
    - DISCONTINUED Product
- Microsoft 16-bit Compilers (C/C++ 7.0 and Visual C++ 1.5)
    - with PharLap 286 DOS-Extender
    - allows access up to 16 MB
- Borland 16-bit and 32-bit
  (C/C++ 4.0 for DOS, Windows and Windows N/T)
    - with PharLap 286 DOS-Extender
    - allows access up to 16 MB
    - with PharLap 386 DOS-Extender (TNT 6.1)
    - allows access up to 4 GB

Future releases to be announced will include:

- Microsoft 32-bit Compiler (Visual C++ 32-Bit Edition)
    - with PharLap 386 DOS -Extender (TNT 6.1)
    - allows access up to 4 GB

2.7.4 Utility Software

SCRAMNET DIAGNOSTICS

The **SCRAMNet** Network Hardware Diagnostics are designed to test the functionality of the hardware. This suite of tests will detect whether it is testing a **SCRAMNet Classic** board or a **SCRAMNet-LX/SCRAMNet+** board and adjust the test menus accordingly.

EEPROM INITIALIZATION (EPI)

The EEPROM Initialization utility is used to simplify configuration of the **SCRAMNet+** network node. The EPI program stores a start-up configuration in the serial EEPROM which can initialize the node on power up. This initialization program can be run when the board is installed to set the desired power-up state of the **SCRAMNet+** node. EPI is completely menu driven and contains a context-sensitive help feature.

SCRAMNET MONITOR

The **SCRAMNet** Monitor allows viewing and editing of memory and CSR locations on the **SCRAMNet+** node. This utility is useful during software development to verify that the correct values are being written to **SCRAMNet+** memory and CSRs.

2.8 Reliability

SYSTRAN Corporate policy is to provide the highest quality products in support of customer's needs. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. The SYSTRAN commitment to quality begins with product concept, and continues after receipt of the purchased product.

SYSTRAN has developed a Quality System which conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard is the most comprehensive of the conformance standards, in that it addresses all 20 clauses of the ISO quality system requirements.

SYSTRAN's Quality System addresses the following basic quality objectives:

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- Improve the quality of its own operations to meet the needs of SYSTRAN customers and stakeholders
- Provide confidence internally that quality is being fulfilled, maintained and improved
- Provide confidence to the customer and other stakeholders that requirements for quality will be achieved in the delivered product.

SYSTRAN's Quality System was assessed by BSI QA, which is the certification division of British Standards Institution, the largest and most respected standardization authority in the world. SYSTRAN's Quality System was found to meet or exceed the international standards in all areas, and Certificate of Registration number FM 31468 was issued to SYSTRAN on May 16, 1995.

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- Professional and quick response to customer problems using SYSTRAN's extensive resources.
- Incorporation of established procedures for product design, test, and production operations, with documented milestones. Procedures are constantly reviewed and improved, ensuring the highest possible quality.

2.9 Technical Support

Technical documentation provided with the product discusses the technology, its performance characteristics, and some typical applications. It includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. SYSTRAN also publishes technical briefs and application notes that cover a wide assortment of topics. The applications selected are derived from real scenarios, but do not cover all possible circumstances.

Direct questions not satisfactorily answered by this document, or concerns about the functional-fit of this product for your particular application, or programming questions, to the factory at **(937) 252-5601**, or send an e-mail message to **support@systran.com** for additional assistance. Our goal is to help solve your problem.

2.10 Ordering Process

If you wish to learn more about SYSTRAN products or to place an order, the following contacts are available:

- Phone: **(937) 252-5601**
- Fax**: (937) 252-2729**
- E-mail address: **info@systran.com**
- World Wide Web address: **http://www.systran.com**

3.0 DESCRIPTION

3.1 Overview

The **SCRAMNet+** Network is a real-time communications network, based on a replicated, shared-memory concept. Each host processor on the network has access to its own local copy of shared memory that is updated over a high-speed, serial-ring network. The network is optimized for the high-speed transfer of data among multiple, real-time computers that are all solving portions of the same real-time problem. The **SCRAMNet+** node board can automatically filter out redundant data.

3.2 Shared Memory

In its simplest form, the **SCRAMNet+** Network system is designed to appear as general-purpose memory. The use of this memory depends only on the conventions and limitations imposed by the specific host computer system and operating system. On most processors, this means that the application program can use this memory in basically the same way as any other data storage area of memory. The memory cannot be used as instruction space.

The major difference between **SCRAMNet+** memory and system memory is that any data written into **SCRAMNet+** memory is automatically sent to the same **SCRAMNet+** memory location in all nodes on the network. This is why it is also referred to as replicated shared memory. A good analogy is the COMMON AREA used by the FORTRAN programming language. Where the COMMON AREA makes variables available to subroutines of a program, **SCRAMNet+** makes variables available to processors of a network.

The **SCRAMNet+** memory size can range from either 4 KB or 128 KB on-board memory to 8 MB of expansion memory. Available options include: 512 KB, 1 MB, 2 MB, 4 MB and 8 MB. Shared memory sizes larger than 128 KB are added using 72-pin **SCRAMNet** memory modules. These memory modules are proprietary and must be ordered from SYSTRAN. A software driver is usually not required except for interrupt handling. When a host computer WRITEs to the shared memory, the proper handshaking logic is supplied by the **SCRAMNet+** node host adapter. The shared memory behaves somewhat like resident or local memory.

3.2.1 Dual Port Memory Controller

The Dual Port Memory Controller (see Figure 2-1) allows the host to READ from or WRITE to shared memory with a simultaneous network WRITE to shared memory. Unless an interrupt has been authorized for that memory address, the host is not aware the network is writing to shared memory. This is why caching must be disabled for **SCRAMNet** memory. If an interrupt has been authorized, the interrupt will then be sent to the host processor.

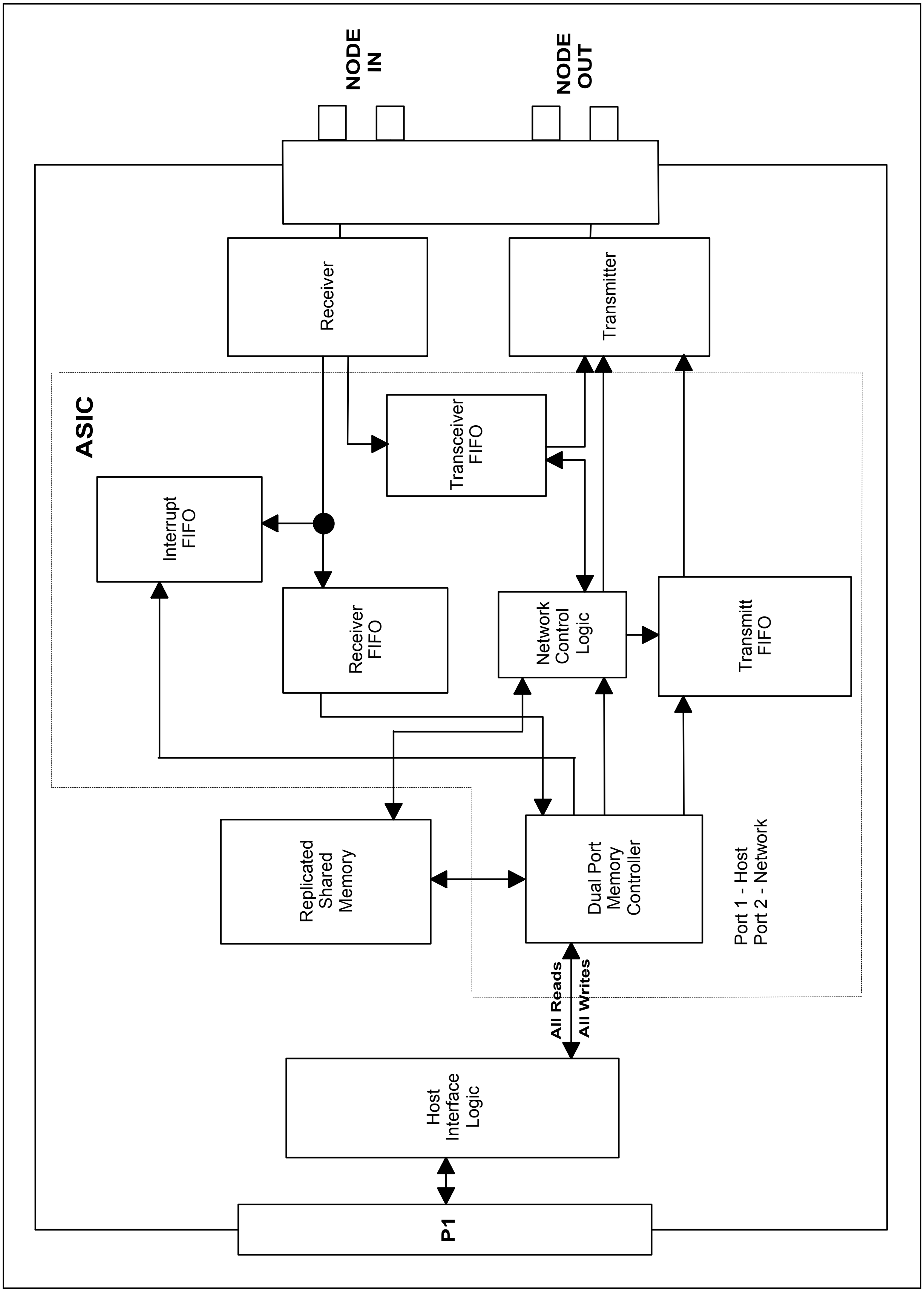


Figure 3-2 Functional Diagram

3.2.2 Control/Status Registers (CSRs)

The operation of the **SCRAMNet+** board is controlled by Input/Output (I/O) CSRs. The location of the CSRs in the computer's address space is software-controlled. In most cases, the mode of operation is set during initialization and remains unchanged during run time. The CSRs are described in detail in Section 5.0 CSR DESCRIPTIONS.

3.2.3 Virtual Paging

The **SCRAMNet+** network may include a variety of **SCRAMNet+** nodes having varying amounts of shared memory. All **SCRAMNet+** nodes use the same 8 MB shared memory map. This feature permits different **SCRAMNet+** boards with 4 MB of shared memory or less to be paged into different sections of the 8 MB memory map. A board with a 4 MB or smaller memory may be located on any shared-memory address boundary that is an even multiple of itself (e.g. 2 MB can page to 0, 2, 4 or 6 MB address).

3.3 FIFO Buffers

The **SCRAMNet+** board contains various FIFO buffers used for temporarily storing information during normal send and receive operation of the node. Refer to Figure 3-2.

3.3.1 Transmit FIFO

The Transmit FIFO is a message holding area for native messages waiting to be transmitted. Each host write to **SCRAMNet+** memory may constitute a WRITE to the Transmit FIFO. (Data Filtering and HIPRO features may interfere with this.) Each WRITE to the Transmit FIFO contains 21 bits of address (A22-A2), 32 bits of data, and one bit of interrupt information. The Transmit FIFO can hold up to 1024 writes before becoming full.

When the Transmit FIFO reaches a FULL condition (CSR1[0] ON), one more host WRITE could cause a message to be lost. To prevent this, the CSR-controllable, built-in **SCRAMNet+** feature called Holdoff mode extends the computer WRITE cycle until the Transmit FIFO is able to empty at least one message.

3.3.2 Transceiver FIFO

This buffer is used to receive foreign messages from the network, and send them on, or to hold received foreign messages while inserting a native message from the host onto the network.

Each node is responsible for receiving foreign messages, writing them to its copy of shared memory, and re-transmitting the message to the next node.

3.3.3 Interrupt FIFO

The Interrupt FIFO contains a 21-bit address (A22 - A2) and a retry status bit for each shared-memory-based interrupt received. The Interrupt FIFO can hold 1024 interrupt addresses. This FIFO can be read using CSR4 and CSR5.

3.3.4 Receiver FIFO

The Receiver FIFO is designed as a temporary holding place for incoming foreign messages while the shared memory is busy servicing a host request. This FIFO is three messages deep, and is designed so it can never be overrun. Each item in the Receiver FIFO contains 21 bits of address (A22 - A2), 32 bits of data, and one incoming interrupt bit. When the messages are 1024 bytes, the initial header information data stays in the

FIFO, the subsequent four bytes of data are loaded in, and the address is incremented by four.

3.4 Network Ring

The **SCRAMNet+** Network is a ring topology network. Data is transmitted at a rate of 150 Mbits/s over dual fiber-optic cables. The two lines together produce the incoming data clock. Due to the network speed and message packet size, the network can accommodate over 1,800,000 message packets passing by each node every second. There is an approximate 247 ns (minimum) delay at each node as the message packet works its way around the ring. The maximum delay depends on the selection of fixed or variable-length message packets. Maximum delay for a fixed-length message packet is 800 ns, it is 16.2 µs for a 256-byte variable-length message packet , and is 62 µs for a 1024-byte variable-length message packet. Delay can be imposed when a node must complete the transmission of a native message packet before retransmitting a foreign message packet. A **SCRAMNet+** Network can accommodate up to 256 nodes per network ring.

3.4.1 Protocol

The protocol is a register-insertion methodology and is <u>NOT</u> a token ring. Depending on the protocol selected, all message packets are the same size or are variable (as in the PLUS modes), and multiple nodes can transmit data simultaneously. There is no master node, and all nodes have equal priority for network bandwidth. The message protocol is designed specifically for real-time applications where data must be passed very rapidly. When the node operates in BURST or BURST PLUS mode, the node will never re-transmit its own messages for error correction. When operating in PLATINUM or PLATINUM PLUS mode, error detection is enabled, and re-transmission can occur.

BURST MODE

BURST mode is an open loop, non-error-corrected communication mode. This mode allows multiple 82-bit messages (46-bit header plus 32-bite data and four parity bits) per node on the ring at a time. The limited message-packet length enhances the data latency characteristics of the network by providing the shortest possible media access delay. The messages are transmitted as fast as the system will allow.

PLATINUM MODE

PLATINUM mode is BURST mode with error correction enabled. The messages are transmitted as fast as the system will allow, but error checking is used to detect and re-transmit corrupted packets.

PLUS MODES

The PLUS mode protocol enhancement can increase the maximum network throughput from 6.5 MB/sec to approximately 15.2 to 16.7 MB/sec by the use of variable-length message packets. Each **SCRAMNet+** message packet has a 46-bit header plus the data. The user-selectable maximum packet size increases the data size from the normal 32 bits to either 256 or 1024 bytes of data. Data must be written to sequential longword addresses.

3.5 Auxiliary Control RAM (ACR)

The Auxiliary Control RAM (ACR) provides a method of external triggering and interrupt control by offering a choice of four actions to occur when a particular **SCRAMNet+** shared-memory address is written into. Each shared-memory location has its own action or set of actions associated with it.

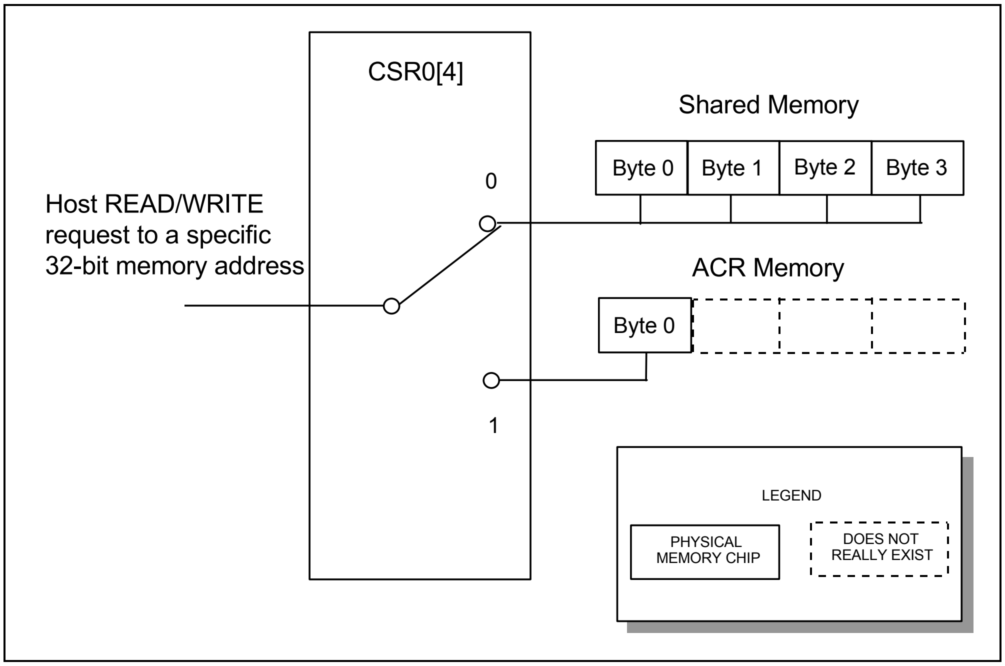


Figure 3-3 ACR/Memory Access

In Figure 3-3, host CPU READ/WRITE operations are channeled to either **SCRAMNet+** memory or to the ACR. The ACR is a physically separate memory from the shared memory. Channeling is based on a user-controlled switch setting and may be toggled to the desired position by writing to a bit in the **SCRAMNet+** CSR. When access to the ACR is enabled, shared memory is not accessible by the host and the ACR byte is viewed as the least significant byte (LSB) of every shared-memory four-byte address. The ACR bits define what external trigger and/or interrupt action(s) are to be taken whenever writing to any byte of the **SCRAMNet+** shared memory 4-byte word.

Only five bits of the ACR are associated with every four-byte word of shared memory (on even four-byte boundaries). The other 27 bits of the ACR are phantom bits and do not physically exist.

☞ **NOTE**: The five writable ACR locations will vary depending on the byte-swapping mode being used by **SCRAMNet**. Refer to subsection 3.11 on Byte Swapping

3.6 Interrupts

SCRAMNet+ allows a node processor to receive interrupts from and transmit interrupts to any node on the network, including the originating node, provided the receiving node is set up to receive an interrupt message. Interrupts can be generated under two different conditions:

- **SCRAMNet+** Network data WRITEs to shared memory; and
- **SCRAMNet+** network errors detected on the local node.

3.6.1 Network Interrupt WRITEs

FOREIGN MESSAGE

The node can receive a message from another node with the interrupt bit set. If Receive Interrupt Enable ACR[0] and Interrupt Mask Match Enable CSR0[5] are enabled, the data is written to shared memory and the address is placed on the Interrupt FIFO.

NATIVE MESSAGE

If the message received was originated by the node, and Write Own Slot Enable CSR2[9] and Enable Interrupt on Own Slot CSR2[10] are enabled, the host has authorized a Self-Interrupt. The data is written to shared memory and the address is placed on the Interrupt FIFO.

Network Interrupt WRITEs can be accomplished by two methods:

- **Selected**. Data WRITEs to selected shared-memory locations from the network.
- **Forced**. Any data WRITEs to any shared memory from the network.

In either case, the node can be configured to WRITE to itself. This condition is called "Self Interrupt" .

3.6.2 Selected Interrupt

The selected-interrupt method requires choosing **SCRAMNet+** shared-memory locations on each node to receive and/or to transmit interrupts. These shared-memory locations may also be used to generate signals to external triggers. The procedure for selecting shared-memory locations for interrupts and/or external triggers is explained in the paragraph on the Auxiliary Control RAM, paragraph 3.5.

OUTGOING INTERRUPT

The Outgoing Interrupt is described in Figure 3-4. If both Transmit Interrupt Enable ACR[1] and Network Interrupt Enable CSR0[8] are set, and a data item is transmitted to any of the selected-interrupt memory locations, then an interrupt message is sent out on the network. This message will generate interrupts to any processors on the network that have that same shared-memory location selected to receive interrupts.

INCOMING INTERRUPT

Figure 3-5 demonstrates the process of receiving a message with the interrupt bit set. The data is written to shared memory and the address is placed in CSR5 and CSR4 to await being sent to the host. If the Receive Interrupt Enable ACR[0], Host Interrupt Enable CSR0[3], and the Interrupt Memory Mask Match Enable CSR[5] are set, and network interrupt data is received for any one of the selected-interrupt memory locations the following occurs:

- the data is stored in that location
- the **SCRAMNet+** address of the memory location is placed on the Interrupt FIFO queue, and
- an interrupt is sent to the processor.

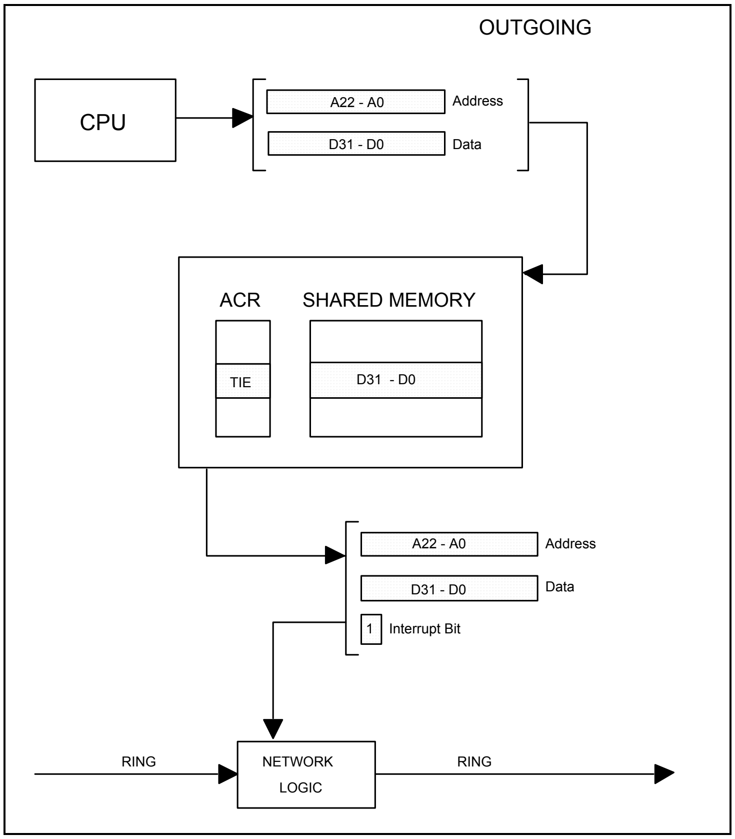


Figure 3-4 Outgoing Interrupt

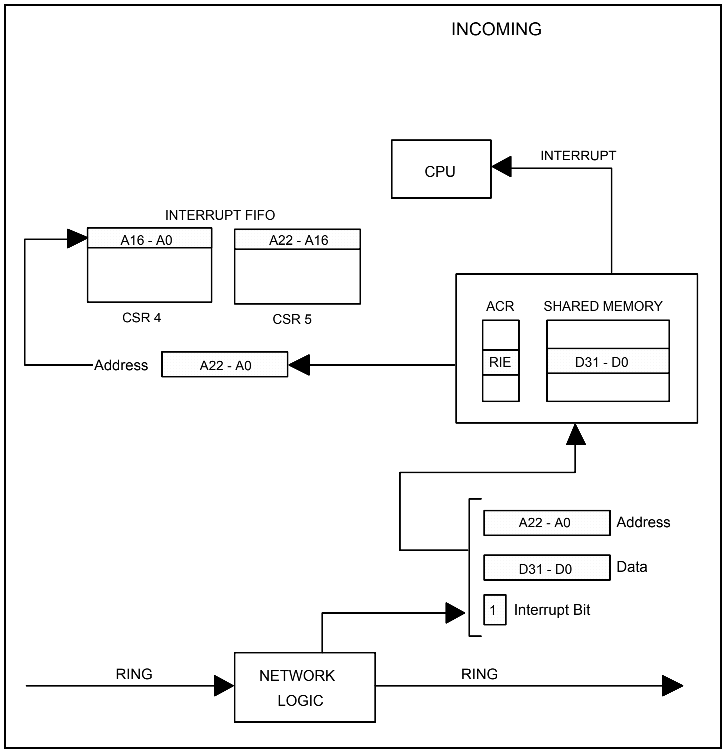


Figure 3-5 Incoming Interrupt

NETWORK ERRORS

The Interrupt on (Network) Errors mode is enabled by setting CSR0[7] ON. Network errors are defined in CSR1 according to an interrupt mask set in CSR9. When an incoming foreign message generates an interrupt, there is no way to mask the interrupt according to the content of the message. However, specific error conditions may be identified.

Error conditions are listed in CSR1 and may be masked by setting the corresponding bit in CSR9. If the Mask bits in CSR9 are all set to '1', any error will generate an interrupt. Otherwise, only errors with a '1' in the appropriate Mask bit will generate an interrupt.

A Network Interrupt vector may be placed in CSR7 to identify a Network Error Interrupt Service Routine.

3.6.3 Forced Interrupt

The forced-interrupt method works the same as for selected-interrupt except for the choice of interrupt locations. All shared-memory locations are automatically set up to receive and/or transmit interrupts depending upon the ACR override conditions set in CSR0[6] and/or CSR0[9].

When Override Receive Interrupt Enable CSR0[6] is set an interrupt will be sent to the host by any network interrupt data message , regardless of the status of the ACR Receive Interrupt bit.

When Override Transmit Interrupt Enable CSR0[9] is set an interrupt will be sent out on the network regardless of the status of the ACR Transmit Interrupt bit.

A third condition, Receive Interrupt Override CSR8[10], is used to designate all incoming network traffic as interrupt messages. The network message interrupt bit does not need to be set.

3.7 External Triggers

Two external triggers are supported by **SCRAMNet+** ISA. The external triggers will occur only if the ACR has been configured to enable them. Triggers 1 and 2 are generated by **SCRAMNet+** shared-memory access. Both triggers generate a 26.64 ns TTL level compatible, non-terminated, output.

- **Trigger 1** - Host Read/Write (ACR[2] enables)
- **Trigger 2** - Network Write (ACR[3] enables)

3.8 General Purpose Counter/Global Timer

The General Purpose Counter/Timer has six modes of operation controlled by CSR8 and CSR9, the output from the General Purpose Counter/Timer is stored in CSR13. Counter modes can count errors, external trigger events, or network messages. A high-resolution timer mode can run free or measure the ring time with a 26.66 ns resolution.

The global timer mode clocks with a resolution of 1.706 µs and resets on an external trigger event. (See 3.7: External Triggers). A specific shared-memory location may be identified with External Trigger 2 ACR[3] so that a memory WRITE from a single node on the network can simultaneously reset all the global timers in the ring.

If the Trigger 2 event is the frame counter, the timers in the ring effectively become synchronized sub-frame timers, which can then be used to tag time-critical data or to measure and compare the completion time of various tasks within a distributed real-time system.

3.9 LED Status Indicators

3.9.1 Network Access

INSERT LED

The green Insert LED is ON when the node is Inserted into the **SCRAMNet+** Network ring.

CARRIER DETECT LED

The green Carrier Detect LED is ON when there is a valid pair of transmit lights from the previous **SCRAMNet+** node into this node's receiver pair. Assuming at least one node is inserted in the ring, if the fiber-optic cables are connected and the Carrier Detect LED is OFF, then the ring integrity is NOT valid. This condition indicates improper fiber-optic cabling or problems with the down-line node's transmitter(s).

3.9.2 Internal Access

A set of eight bi-color LED indicators are available for troubleshooting and fine tuning of the node. Since there are no remote sensors, the chassis must be open to observe the LEDs.

Four “HOST” LEDs indicate READ and WRITE transactions to shared memory or to control/status registers, an indicator to show receipt of a host acknowledgment, and indication of a memory or CSR interrupt.

Four “NETWORK” LEDs show message waiting; and receipt of an error, a foreign message, or a native message.

3.10 Modes of Operation

3.10.1 Data Filter Mode

When **SCRAMNet+** Data Filtering is enabled, only those WRITEs to **SCRAMNet+** memory that produce a data change are transmitted to the network.

EXAMPLE:

If location 1000 in **SCRAMNet+** memory contains the value ‘20’ and the host processor WRITEs the value ‘20’ to location 1000, then no network traffic will be generated. However, if any other value is written to location 1000, then the new value will be passed around the network to update the other **SCRAMNet+** node memories.

When a WRITE is received from the host, a comparison is made to the old data at that address to see if there was a change before writing to shared memory. If the data has changed, then it is written to shared memory, and is also transmitted onto the network. This entire process is completed within the host memory standard bus WRITE cycle.

Data filtering is a powerful communications compression technique for cyclical applications. This technique has been shown to significantly reduce the network traffic and therefore increase the effective throughput on the network.

3.10.2 High Performance (HIPRO) Mode

HIPRO provides an efficient means to transmit 8-bit and 16-bit data transactions as one 32-bit network WRITE. It also provides a means of keeping 32-bit data from becoming fractured.

EXAMPLE #1:

A floating point length numeric sent in 8-bit or 16-bit pieces may not be accurately re-assembled at the destination.

EXAMPLE #2:

The receiving node may otherwise try to use part or half of such a value before the entire 32 bits is received.

HIPRO WRITE

The **SCRAMNet+** network message is based on 32-bit longword data. This means if any 8-bit field of the 32-bit buffer is changed, the entire 32-bit message is transmitted. If a host is limited to only 8-bit or 16-bit databus transactions the network throughput is quartered or halved, respectively.

HIPRO mode permits a 32-bit location to be set up in shared memory such that any initial WRITE smaller than 32 bits to that location will not automatically go onto the network. The 32-bit WRITE to the network will only occur when all four bytes within the 32-bit location have been written through subsequent WRITEs by the host CPU. This can be accomplished by four consecutive 8-bit or two consecutive 16-bit WRITEs to the **SCRAMNet** memory.

3.10.3 Holdoff Mode

It is possible that the Transmit FIFO can become full when the host is writing to the **SCRAMNet+** interface faster than the network can absorb the data.

In Holdoff mode, the host WRITE cycle is automatically extended until the **SCRAMNet+** Transmit FIFO buffer transmits at least one message. This prevents the loss of data and is transparent to the user.

In some system designs, and on some computer buses, it is not desirable or effective to have the WRITE cycle lengthened to match network throughput—even at the expense of possible data loss across the network. In this case this option may be disabled by setting CSR8[1] ON. Transmit FIFO 7/8 Full CSR1[2] can then be used to control the data flow via software control.

3.10.4 Loopback Modes

Loopback mode is used for testing, and for routing data, which would normally be transmitted onto the network back into the node. This mode is used to check performance internally (Wire Loopback) at the Media Card (Mechanical Switch Loopback) and Transmit/ Receive (Fiber-optic Loopback).

WIRE LOOPBACK MODE

The Wire Loopback mode needs no manual external modifications to work. Wire Loopback is enabled by setting CSR2[7] ON. This mode checks the on-board circuitry for continuity.

NOTE: If a node is inserted into the network while in wire loopback mode, it will create a break in the network ring, making all nodes down-line unreachable.

MECHANICAL SWITCH (MEDIA CARD) LOOPBACK MODE

Mechanical Switch (Media Card) Loopback mode is enabled by setting Mechanical Switch Override CSR8[11] to OFF. This test is used to check the circuitry onto the Media Card but excludes the fiber-optic circuitry. In this test the signal does not leave the Media Card.

FIBER-OPTIC LOOPBACK MODE

The Fiber-optic Loopback mode must have the optional Fiber Optic Bypass Switch connected, Disable Fiber Optics Loopback CSR2[6] set to OFF (power up default), and Insert Node CSR0[15] enabled to be valid. When the Fiber-optic Loopback mode is in effect, the output of the transmitter is connected by fiber optics directly to the input of the receiver, and the receiver is disconnected from the network.

The optional Fiber Optic Bypass Switch must be installed for this loopback to work. However, in the absence of the Fiber Optic Bypass Switch, fiber-optic cables could be run from the node’s transmitter output connectors to the receiver input connectors. This configuration, with Insert Node enabled, would constitute a Fiber-optic Loopback mode for stand-alone testing. Set CSR2[6] ON to disable the Fiber-optic Loopback mode when the node is in use as a part of the network. This configuration is not a substitute for the Fiber Optic Bypass Switch for network operation.

3.10.5 Write-Me-Last Mode

The Write-Me-Last mode of operation allows the originating node to be the last node in the ring to have the data deposited to its memory. This can be useful for synchronization. This means that when the host performs a WRITE to the **SCRAMNet+** shared memory, this data is not immediately written to the host node’s memory, but is first sent to the other nodes on the network. When the message returns to the originating node it is written to shared memory, and is then removed from the network ring.

Therefore, host-originated data written to shared memory travels the ring updating the **SCRAMNet+** node memories on the ring and, upon returning to the originating node, that node WRITEs the data to its own shared memory as the last node on the ring. This guarantees that the data is available on all other nodes.

3.11 Options

3.11.1 Electronic Bypass Switch

The Electronic Bypass Switch exists on some Media Cards. This switch allows for fast bypass on power-fail conditions. The electronic switch operates in the low nanosecond range compared to a 20 millisecond time for a typical mechanical switch.

In case of node power failure, the electronic switch restores the network so quickly that only one or two messages will have to be retransmitted, whereas a mechanical switch could cost an excessive amount of transmission time re-sending perhaps thousands of messages.

3.11.2 Quad Switch

The **SCRAMNet** Quad Switch is designed to provide configuration control over the network topology and computing resources. The Quad Switch allows local clusters of up to four **SCRAMNet** nodes to be switched in or out of a primary **SCRAMNet** ring, independently and dynamically (Figure 3-6). It also allows sharing of a critical real-time resource between multiple systems.

The Quad Switch performs other useful functions such as optical bypassing, fiber-optic repeating to gain transmission length beyond the **SCRAMNet** node's transmission power limit, and to act as a media converter.

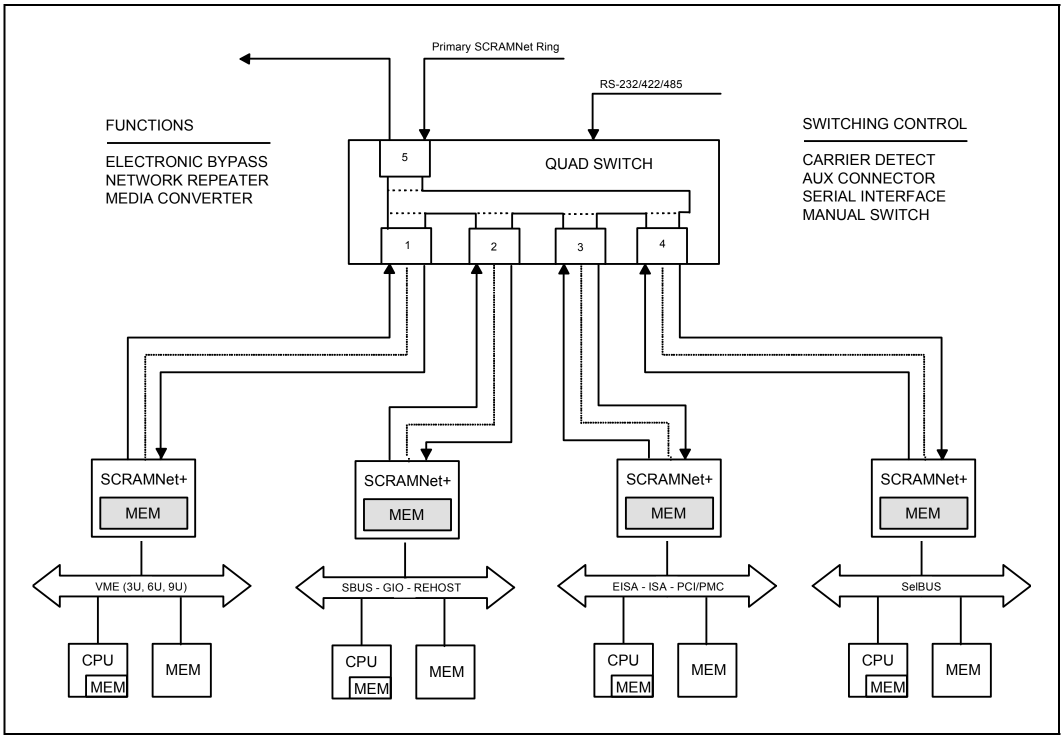


Figure 3-6 Node Inclusion and Isolation

The electronic bypass switching action is very fast, introducing a total network disruption of about one microsecond. This is over 10,000 times faster than mechanical optical bypass switches, and permits ring re-configuration to be performed in real-time with minimal impact on the system.

As a repeater, each Quad Switch port converts optical signals to electrical signals. These signals are re-synchronized and re-transmitted. This allows each connection to the Quad Switch to be the maximum length for the type of media selected.

The Quad Switch can also perform media conversion. Since each port has a Media Card just like a **SCRAMNet** node, each port can be configured to handle coaxial, standard link or long link fiber. This allows a signal to arrive on one media type, and go out on another.

Visually, LED's signify the state of node inclusion in the ring and if carrier is detected. If carrier is not detected, the port is put into Isolate state and the port is bypassed thereby retaining ring integrity. The auxiliary connector and the associated control cable links the port to the node to allow the application running the node to switch the Quad Switch in and out of Include or Isolate state. A manual Include/Isolate switch is used to guarantee that a node is isolated or that it can be included. A serial port interface is used to send message packets to the Quad Switch to perform control functions or to obtain switch status remotely via the RS-232 or RS-422/485 connection. Two mechanical rotary switches set the serial interface address.

4.0 INSTALLATION

4.1 Installation Procedures

Installation of the ISA board includes the following:

- Unpack the board
- Visually inspect the board
  - Check SIMM connection
  - Check Media Card connection
- Configure the Board
  - External Triggers
  - Select PnP/non-PnP Device Activation Option
- Install the board
- Select Cabling Options
- Install Fiber Optic Bypass Switch (optional)
- Install the software
- Internally Configure the board
  - Map ISA Register Addressing
  - Set up **SCRAMNet+** ISA Registers
  - Set up **SCRAMNet+** Control/Status Registers
  - Select message length option
  - Select software compatibility option
  - Set Node Identification (CSR3[15:8])
  - Set Network Time-out (CSR5)
  - Set Memory Base Address (CSR10[15:12] and CSR11[15:0]
  - Enable Shared Memory (CSR10[0])

4.2 Unpack the Board

Perform the following steps:

- The ISA host card is wrapped in an anti-static bag and encased in anti-static foam.

CAUTION: Use an anti-static mat connected to a wristband when handling or installing the **SCRAMNet+** board.

- Remove the ISA anti-static bag from the carton.
- Open the anti-static bag and remove the ISA host card.

Save the shipping material in case the **SCRAMNet+** board needs to be returned.

The optional fiber-optic cables and Fiber Optic Bypass Switch are shipped in separate cartons.

4.3 Visually Inspect the Board

Check the board for any damage that may have occurred during shipping. In the event that any shipping damage has occurred, call SYSTRAN Customer Service at (937) 252-5601.

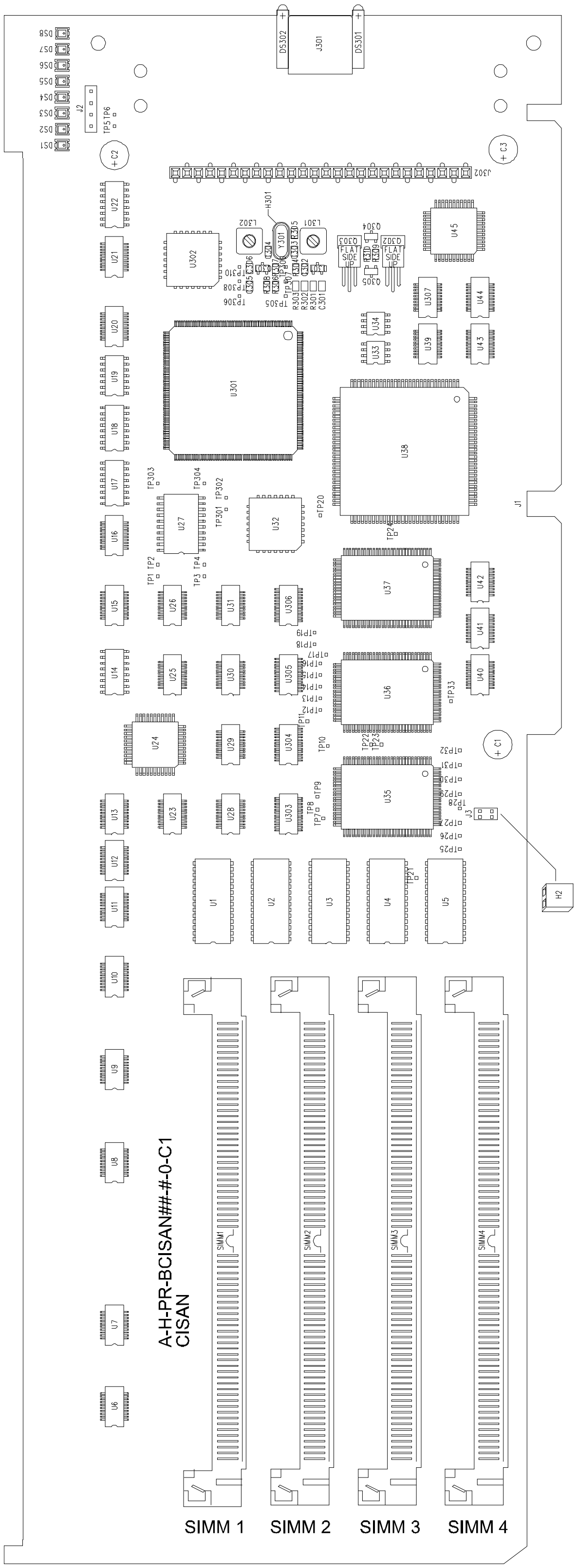
4.4 ISA Board Description

Figure 3-1 represents the **SCRAMNet+** ISA board. The ISA J1 connector plugs into the ISA bus.

Host and Network Internal Access bi-color

External Trigger

Media Card Connection



PnP System Option Jumper (J3)

Part Number & Version

SIMM Connections

Figure 4-7 ISA Layout

4.4.1 Check SIMM Connections

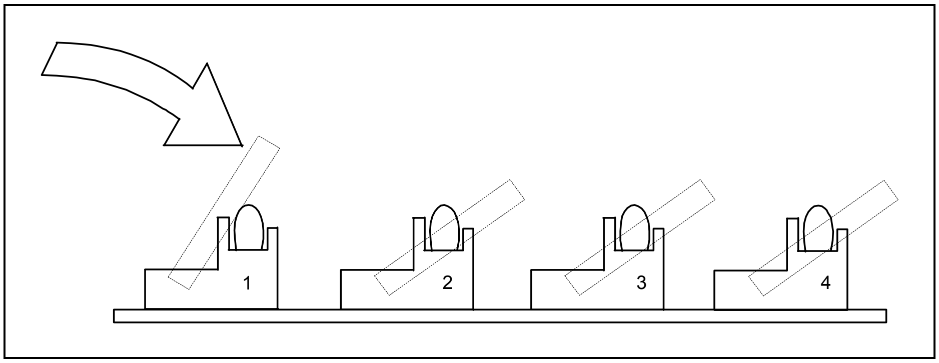


Figure 4-8 SIMM Installation

To install SIMMs, set the SIMM in the slot and gently press back and down until the clips snap into place as shown in Figure 3-2.

To remove the SIMMs, push the clips gently to the outside with each thumb while gently pulling the SIMM toward you with your index fingers.

The SIMMs are proprietary and must be ordered from SYSTRAN. In the case where no SIMMs are installed, shared memory defaults to the on-board 4 KB or 128 KB. If SIMMs are to be installed, these are the following options:

- Low density, 512 KB SIMMs
  1 = 512 KB (SIMM 1)
  2 = 1 MB (SIMM 1 and 2)
  4 = 2 MB (SIMMs 1 through 4)

- High density, 2 MB SIMMs
  1 = 2 MB (SIMM 1)
  2 = 4 MB (SIMM 1 and 2)
  4 = 8 MB (SIMMs 1 through 4)

SIMMs must all be either low density or high density; they cannot be mixed.

4.4.2 Check Media Card Connection

Internal Power (pins 1 & 2)
External Power (pins 2 & 3)

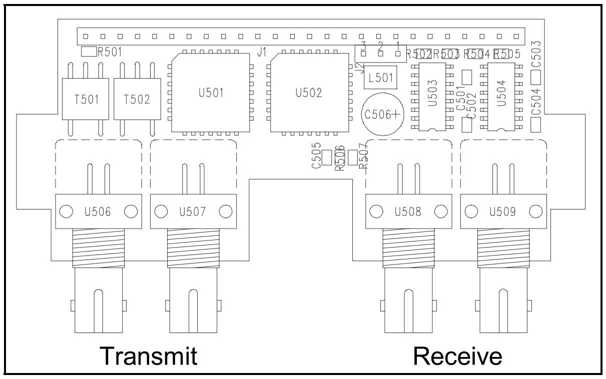


Figure 4-9 Fiber-optic Media Card (Bottom view)

The Media Card can have either coaxial or fiber-optic connectors. Figure 4-9 shows the fiber-optic media card. The **SCRAMNet+** ISA board will support either option. The type of Media Card installed will be dictated by the network configuration. There are two receive connections (Rx1 and Rx2) and two transmit connections (Tx1 and Tx2).

This fiber-optic card has two power options; host power and standby or battery power. Jumper J2 in Figure 4-9 controls the power options. Pins 1 and 2 are for normal host power, and pins 2 and 3 are for standby power. The standby or battery power requires external connection via the auxiliary connection on the cabinet kit board or the host interface board if no cabinet kit is installed.

4.5 Configure the Board

4.5.1 External Triggers

The **SCRAMNet+** board generates two external triggers. Activating the triggers for any **SCRAMNet** memory location will cause an external trigger to be generated when the **SCRAMNet** memory location is accessed (Figure 3-9, Tables 3-5, 3-6).

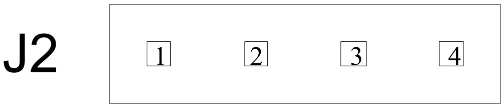


Figure 4-10 External Trigger Connections (J2)

Table 4-1 Trigger Pin Connections (J2)

Pins	Output
1	TRIG2
2	TRIG1
3	TRIG1 or TRIG2
4	GROUND

Table 4-2 External Trigger Actions

Trigger	ACR	Action
1	bit 2	Host READ/WRITE
2	bit 3	Network READ/WRITE

4.5.2 Select Device Activation Option

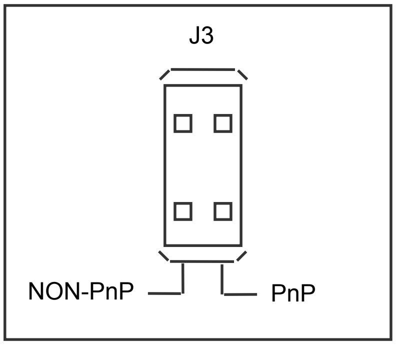


Figure 4-11 System Option Jumper (J3)

PNP SYSTEM

If the host system has a plug-and-play BIOS, it doesn’t matter how J3 in Figure 4-11 is set.

Activate the board using software by running **scr_cm -activate.**

NON-PNP SYSTEM

If J3 is set to “PnP”, activate the board using **scr_cm -activate**.

If J3 is set to “Non-PnP” the device acts like a normal ISA board, and is active upon boot-up.

CONFIGURATION

Configure the board using the Configuration Manager software (**scr_cm**). Initially this sets up the **SCRAMNet+** ASIC PnP EEPROM.

The diagnostic and/or Monitor software can be run at any time.

NOTE: To insure proper timing delays in the programming of the digital switch components on the **SCRAMNet** board, and to avoid conflict with Windows when the program scans upper memory to detect the presence of PnP BIOS, the **scr_cm** program must only be run from DOS—not under Windows.

4.6 Install the Board

CAUTION: Make certain that the power to the host computer is OFF.

1. Remove the cover from the host machine.
1. Remove the bulkhead cover plate where the **SCRAMNet+** host card will be.
1. Install the host card into the ISA bus slot.
1. Connect the Transmitter and Receiver fiber-optic cables to the **SCRAMNet+** card.

4.7 Select Cabling Options

Options include installation of coaxial or fiber-optic cable. Media cards can be ordered for either one.

4.7.1 Coaxial Cable Configuration

SCRAMNet+ coaxial cable is composed of paired, shielded conductors terminated with SMA connectors. Maximum node separation using coaxial is 30 meters. The recommended coaxial cable is RG-58.

4.7.2 Fiber-optic Configuration

The basic **SCRAMNet+** Network communication architecture consists of **SCRAMNet+** boards tied together by paired sets of fiber-optic cable in a ring configuration. The maximum recommended distance between each node of the network using this configuration is approximately 300 meters. Maximum node separation using long-link fiber is 3,500 meters. The recommended fiber-optic cable is 62.5/125 micron core multi-mode fiber cable with ST connectors.

NOTE: On a freshly powered system, a message from any node on the ring may be necessary to establish the carrier.

4.7.3 Fiber-optic cables

The optional paired fiber-optic cables are shipped in a separate carton. The fiber-optic cables are to be attached to the connectors on the **SCRAMNet+** board or on the Cabinet Kit, as appropriate. Remove the rubber boots on the fiber-optic transmitters and receivers as well as the ones on the fiber-optic cables. These rubber boots should be replaced when cables are not in use or in the event the node must be returned to the factory.

It is important that the ends of the fiber-optic cable be kept clean. If there is an exceptional amount of light-power loss experienced, the cable ends should be inspected for cleanliness. Alcohol-based fiber-optic cleaning pads are available to remove minor contaminants such as dust and dirt.

Figure 4-12 is a representation of a fiber-optic connector.

FIBER-OPTIC CABLE PRECAUTIONS

Fiber-optic cables are made of glass and may break if crushed or bent in a loop with less than a 2 inch radius.

Perform a visual check of the cable ends before inserting into the Media Card connector. If debris is inserted into the transmitter/receiver connector it may not be possible to clean it out or could result in damage to the transmitter or receiver lens. Hair, dirt and dust can interfere with the light signal transmission.

Use an alcohol-base wipe to clean cable ends.

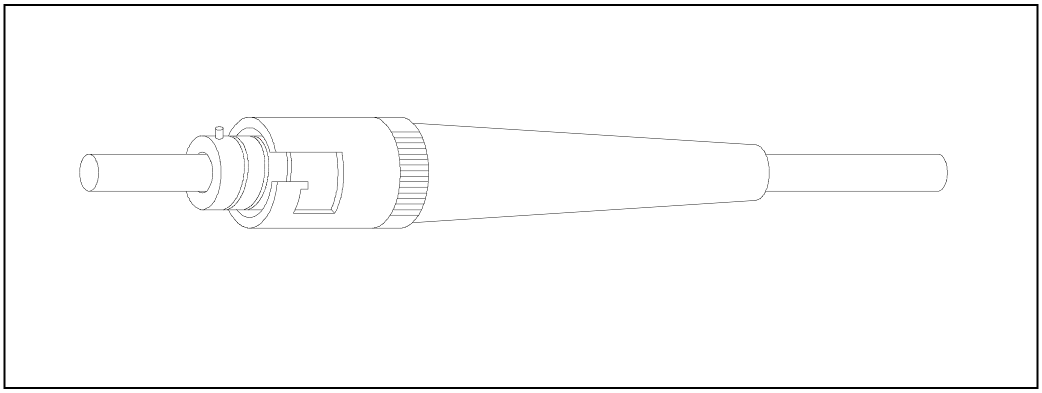


Figure 4-12 Fiber-optic ST Connector

4.7.4 Fiber-optic connection

The fiber-optic cable pairs should be connected between the transmitter pair of the down-stream node and the receiver pair of the up-stream node. Continuing this type of connection to all nodes in the network will result in a daisy-chain-network ring as indicated in Figure 4-13.

NOTE: It does not matter if Tx$_1$ or Tx$_2$ is connected to the next node's Rx$_1$ or Rx$_2$ as long as both Tx cables are connected to both of the next node's Rx connectors

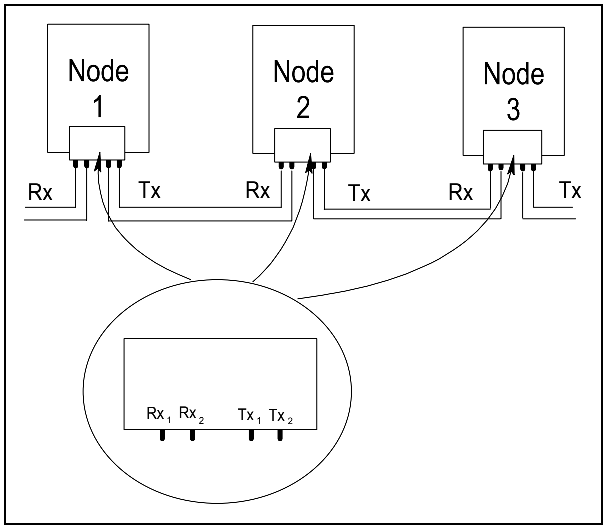


Figure 4-13 Fiber-optic connections

4.8 Install Fiber Optic Bypass Switch (Optional)

Make Fiber Optic Bypass Switch connections as shown in Figure 4-14 and Figure 4-15.

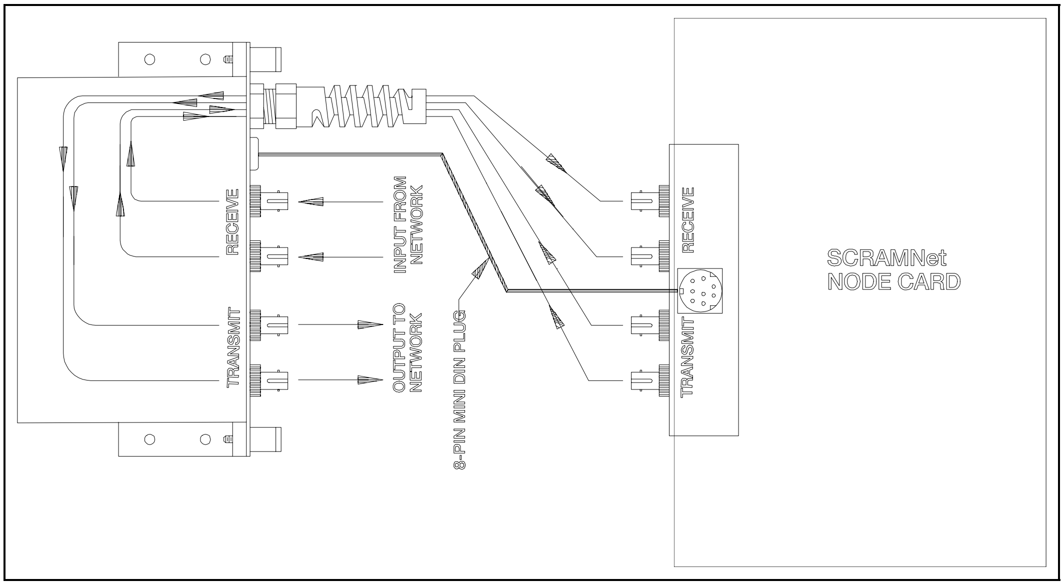


Figure 4-14 Inserted State (Power On)

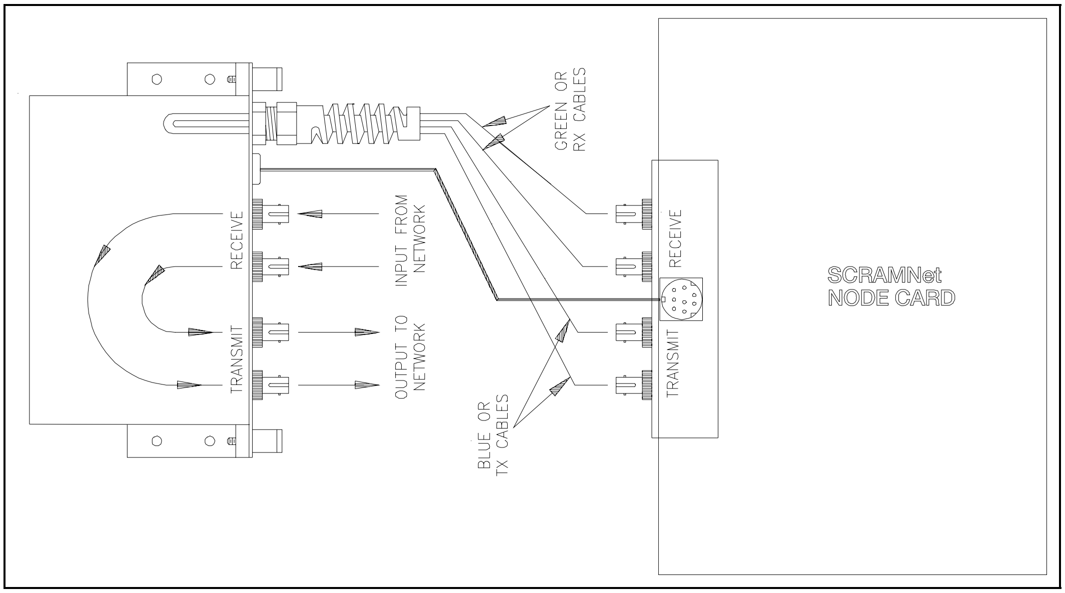


Figure 4-15 Bypass State (Power Off)

4.8.1 Auxiliary Connection

The Auxiliary Connection at the Media Card is used for communication with the Fiber Optic Bypass Switch. The 8-pin modular in-line plug male-pin connection described in Figure 4-16 is defined in Table 4-1. (The view is looking into the connector).

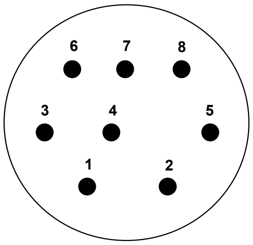


Figure 4-16 Auxiliary Connection

Table 4-1 Auxiliary Connection Pinout

Pins	Name	Definition
1	GND	Logic Ground
2	S_CLK	Serial Clock
3	F_RELAY	Fiber-optic Relay Drive and Sense
4	S_DATA	Serial Data
5	EXT_PWR	+5 Source to External Ground
6	S_DIR	Serial Data Direction
7	TRIGGER	Trigger Output (TRIG1)
8	BAK_PWR	Backup +5 Source from External Device

4.9 Install the Software

Install the **SCRAMNet+** software in accordance with instructions in the *SCRAMNet Software Installation manual.*

4.10 Internal Configuration

The SCRAMNet Configuration Manager software must be installed in order to complete the ISA board configuration. Refer to the *SCRAMNet Software Installation Manual for ISA*.

4.10.1 SCRAMNet+ Control/Status Registers (CSR)

Table 4-2 is a listing of the **SCRAMNet+** Control/Status Registers and their ISA addresses (Base address + offset).

Table 4-2 SCRAMNet+ Control/Status Registers

ISA Address	Alias	Size (Bytes)	Active Bits	Type	Register Description (contiguous through 0z020H)
0	CSR0	2	16	R/W	General SCRAMNet+ Enable and Reset
2	CSR1	2	16	R/W	SCRAMNet+ Error Indicators
4	CSR2	2	16	R/W	General SCRAMNet+ Control
6	CSR3	1 1	8 8	R/W R/W	Number of nodes Node ID
8	CSR4	2	16	R	Interrupt FIFO Address (LSW)
A	CSR5	2	9 7	R[1] -	Interrupt FIFO Address (MSW) Reserved[2]
C	CSR6	2	8	-	ISA Transfer Register
E	CSR7	2	0	-	Reserved[2]
10	CSR8	2	16	R/W	Extended Control Register
12	CSR9	2	16	R/W	Interrupt On Error Mask
14	CSR10	2	0	-	Reserved[2]
16	CSR11	2	0	-	Reserved[2]
18	CSR12	2	16	R/W	Virtual Paging Register
1A	CSR13	2	16	R/W	General-purpose Counter/Timer
1C	CSR14	2	10	-	ISA Page Select Register
1E	CSR15	2	0	-	Reserved[2]

NOTES: 1. WRITE Transmit Time-out to shadow memory
2. Reserved registers may contain random data. Do not be concerned.

4.10.2 EEPROM Initialization

The EEPROM is used to store the initial power-up register values. The EEPROM can be programmed either over the host backplane or by most PROM programmers. An EEPROM initialization (EPI) program is included in the SYSTRAN Software Utilities Package for most systems.

The board comes with power-up default values in each of the registers and default switch settings so the board can be used without making any changes. Defaults are shown in Table 4-3 where 000 = CSR0, 002 = CSR1, 004 = CSR2. Both location 006 and 008 write to CSR3, TX_ID,RX_ID. This is possible because CSR4 is READ Only. Then location 00A = CSR5, etc.

Table 4-3 EEPROM Table

	0	2	4	6	8	A	C	E
00	0000	0000	C040	XX00	XX00	0010	0003	0000
10	0800	0FF0	0000	0000	0000	0000	0000	0020
...	0000	0000	0000	0000	0000	0000	0000	0000
70	5555	5555	5555	5555	5555	5555	5555	5555

NOTE: XX denotes TX_ID and RX_ID. Both values are the same.

These values are assigned to the Control/Status Registers on power-up. The values may be changed at any time using the appropriate software to access the CSRs. When the system is powered down and powered up again, the CSRs will be reinitialized to these EEPROM values. Only the first 16 values are used in the registers. Table 4-4 describes the default value and function.

Table 4-4 EEPROM Initialization

SCRAMNet+ Registers	
CSR0 - 0	CSR1 - READ Only (Errors)
CSR2 - 0xC040 (BURST Mode)	CSR3 - Node ID (0 - 255)
CSR4 - 0 (READ Only)	CSR5 - 0x0010 READ Only (WRITE a non-zero Network Time-out to shadow register)
CSR6 - 0 (Memory Page Selection/ Byte Swapping Configuration/ Page Enable/SIMM Enable)	CSR7 - 0 (Reserved)
CSR8 - 0x0800 (Mech Switch Override)[$]	CSR9 - 0x0FF0 (Error Mask)[#]
CSR10 - 0 (Reserved)	CSR11 - 0 (Reserved)
CSR12 - 0 (Virtual Page)	CSR13 - (GP Counter)
CSR14 - 0 (ISA Page Select)	CSR15 - 0 (Reserved)

[$] HOLDOFF is enabled

[#] Normal Error Masking enabled

4.10.3 Node Identification

To set the Node ID, WRITE a unique value 8-bit number between 0 and 255 to CSR3[15:8].

CAUTION: Each node in the ring must have a unique Node ID.

4.10.4 Network Time-out

The recommended value for the Network Time-out is:

# NODES IN RING + (TOTAL LENGTH OF CABLE IN METERS÷50) + 1

To set the network time-out value, WRITE the result as a 16-bit hexadecimal number to CSR5. This register has a "shadow register" which holds the network time-out value. Each increment in the "shadow register" is worth approximately 240 ns. The time-out will be 240 ns multiplied by the value written.

The time-out register is WRITE ONLY. If a READ is performed, it will result in a READ to the Interrupt FIFO.

CAUTION: Ensure a non-zero value is written to CSR5. A value of '0' will prevent host-generated data from leaving the Transmit FIFO.

4.10.5 Memory Addressing

The **SCRAMNet+** memory address must begin on an even boundary beyond extended memory pool, where the boundary is a multiple of the installed board memory. There must be a non-contiguous "gap" between system memory and the SCRAMNet+ ISA board shared-memory address. For example, if the system has 6 MB of RAM, and the **SCRAMNet+** ISA board has 8 MB of SIMMs, the address for the board would be at the 8 MB boundary.

The Least Significant Word (LSW) of shared memory address is in CSR10[15:12]. The Most Significant Word (MSW) of shared-memory address is contained in CSR11[15:0].

4.11 Byte Swapping

Some computer systems use different methods of byte ordering. Some have the high bytes arranged from right to left (Little Endian) and others have the high bytes going from left to right (Big Endian). Motorola is an example of a Big-Endian system. Intel is an example of a Little-Endian system.

Table 4-5 is a simplified summary for 8-bit, 16-bit, and 32-bit byte ordering for big endian and little endian. This table shows for a big-endian-value written to 8-, 16- or 32-bit memory, the corresponding little-endian equivalent for that sequence of values if read using the same transaction size. Additionally, to ensure data is correctly swapped when reading/writing **SCRAMNet** ISA shared memory, the byte swapper must be set to the same transaction size as that being sent to the **SCRAMNet** ISA card.

Table 4-5 Byte Ordering Comparisons

Size	Big Endian	Little Endian
byte (8-bit)	12 34 56 78	78 56 34 12
shortword (16-bit)	1234 5678	5678 1234
longword (32-bit)	12345678	12345678

Byte swapping on the ISA card is controlled by setting CSR6[0] and CSR6[1]. See pages 5-11 and A-6 for more information.

EXAMPLE

To read 16-bit data correctly from the SCRAMNet ISA card, set the byte swapper to 16-bit mode. The same holds true for 8- and 32-bit data.

The **SCRAMNet-LX** and **SCRAMNet+** product line has adopted the big-endian ordering philosophy as the default for data passing. **SCRAMNet-LX** and **SCRAMNet+** do not have a built-in byte-ordering conversion function.

Little-endian ordering may be used when no big-endian-based systems are present.

4.12 Maintenance

No routine maintenance is required for the **SCRAMNet+** general purpose nodes beyond that which is required for host computer systems. **SCRAMNet+** network fiber-optic cabling connectors should be inspected periodically.

4.13 Troubleshooting

On a PC platform there is no power-up indication. If there is an incorrect address, the system will not boot up.

On UNIX-like systems, the driver will output a message on boot-up similar to the following:

```
SCRAMNet+ installed and on-line
```

If this message does not appear, the Register base address, memory base address and/or memory size may be incorrect.

All **SCRAMNet+** nodes in the fiber-optic network ring must be powered on unless they have Fiber Optic Bypass Switches or Quad Switches installed.

4.13.1 Internal Access LED Indicators

LED indicators on the board can be used to assist with troubleshooting or fine tuning of the network node. There are no remote indicators, so the chassis must be left open in order to observe the LEDs.

The bi-color LEDs show either green (G) or yellow (Y) .

As shown in Figure 4-17, the LEDs are divided into two groups—HOST and NETWORK.

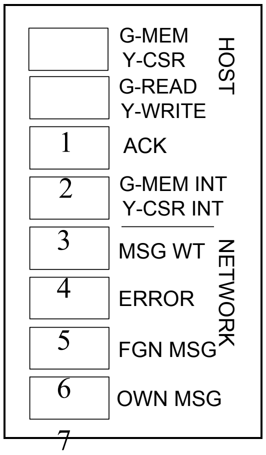


Figure 4-17 LED Indicators

HOST

LED 1 and LED 2 are viewed together to indicate a memory/CSR READ or WRITE as shown in Table 4-6.

Table 4-6 LED 1 and LED 2 Definitions

Action	Memory		CSR	
	LED 1	**LED 2**	**LED 1**	**LED 2**
READ	G	G	Y	G
WRITE	G	Y	Y	Y

LED 3 indicates a Host Acknowledge signal has been received.

LED 4 (G) indicates a memory interrupt has been received.
LED 4 (Y) indicates a CSR interrupt has been received.

NETWORK

LED 5 indicates a message is waiting to be transmitted.

LED 6 indicates an error condition set in CSR1 has been detected.

LED 7 indicates a foreign message has been received.

LED 8 indicates a native (OWN) message has been received.

4.13.2 Hardware

The following hardware conditions will cause the installation to fail:

- The **SCRAMNet+** ISA host card is not installed into a standard ISA slot. (This check should have been performed before installing the **SCRAMNet+** ISA host card into any slots).

4.13.3 Customer Support

If the system does not boot correctly, reseat the board and double-check cable connections. If problems persist, call SYSTRAN Customer Support at (937) 252-5601 for assistance.

Be prepared to supply the following information:

Host machine: ______________________________
OS Name: ______________________________
OS Version: ______________________________
Bus Interface: ______________________________

5.0 OPERATION

5.1 Introduction

The **SCRAMNet+** Network is a shared-memory system. Every computer on the network has a constantly updated local copy of all global data which is passed to all the network computers. The network protocol is implemented in the **SCRAMNet+** hardware and therefore no software overhead is required to retrieve this information from the network.

The protocol is transparent to the computer. This frees computer processor time for application algorithm execution and other real-time tasks. Since any computer on the network has access to data in the shared memory, any computer can read or modify the shared data and thereby communicate with the other computers on the network.

Very little special software is required for normal operation because of the **SCRAMNet+** shared-memory configuration. Typically, **SCRAMNet+** memory is installed and linked to a host global common block through the host operating system. Once the link is complete, any program can reference **SCRAMNet+** memory as a standard common-block variable reference.

For interrupt driven applications, an interrupt service routine (ISR) is required to handle the interrupts triggered by the **SCRAMNet+** node. An example of a generic ISR is included Figure 5-11, page 5-28 at the end of this section.

5.2 Shared Memory

Global variables are mapped directly onto the replicated shared memory. The application program typically contains a list of variables or arrays which are stored in a contiguous space and which are to be shared across processors. The analogy of a FORTRAN COMMON BLOCK is most fitting. For the purpose of identification, these variables are referred to as **SCRAMNet+** variables.

The application program usually requires a short section of instructions to initialize the **SCRAMNet+** hardware and to link the **SCRAMNet+** memory to the **SCRAMNet+** variable list. The shared memory cannot be used as instruction space.

5.2.1 Virtual Paging

CSR12 is the virtual-paging register. Set CSR12[0] to ‘1’ to enable virtual paging.

The **SCRAMNet+** network may include a variety of **SCRAMNet+** nodes having varying amounts of shared memory. All **SCRAMNet+** nodes use the same 8 MB network shared-memory map. Virtual paging allows a node with 4 MB or less shared memory to move its memory window throughout the **SCRAMNet+** physical 8 MB network shared-memory map.

If a node has 4 MB of shared memory, it can be paged into the upper 4 MB or the lower 4 MB of the network shared-memory map. If it is paged into the lower 4 MB, it would operate the same as if Virtual Paging were disabled. The network address would be the same as the shared-memory address.

NOTE: Virtual paging does not affect host access to shared memory. Virtual Paging only changes the network address. The host-specific logic always sees the base address of **SCRAMNet+** shared memory as zero.

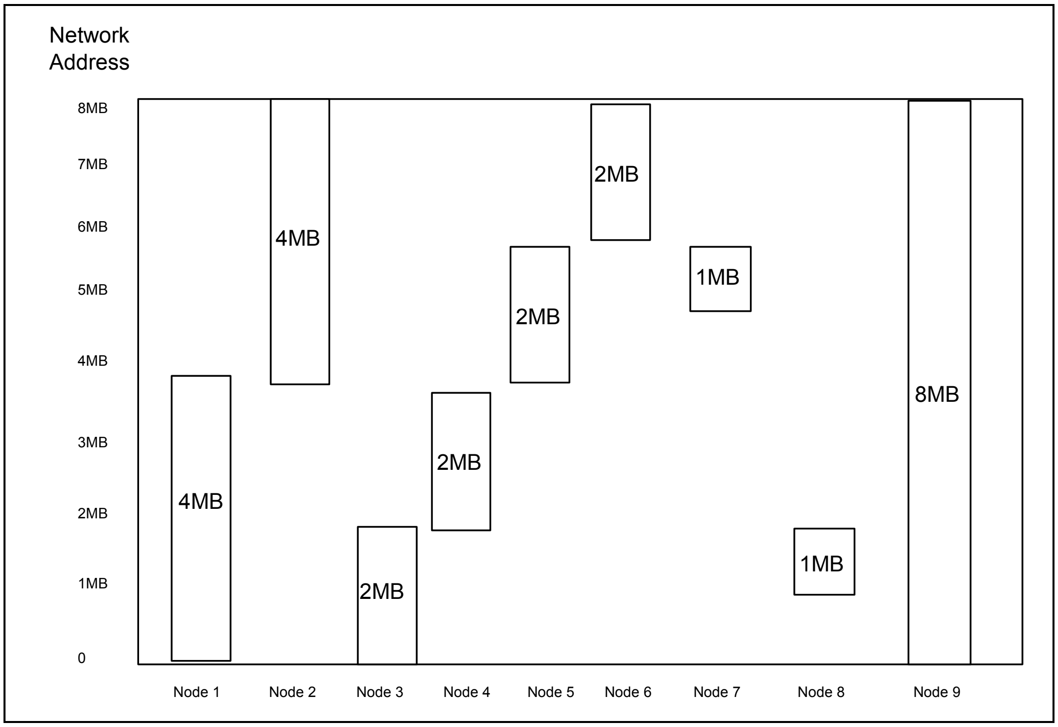


Figure 5-1 Memory Sharing With Virtual Paging

If the 4 MB block were paged into the upper 4 MB, a host-specific WRITE to a shared-memory address of 2 MB would result in a network address of 6 MB. This translation is bi-directional. An incoming network message with a network address of 6 MB will be written to shared memory at 2 MB. Any WRITE accesses to the lower 4 MB will be ignored since there is no memory addressed there.

To produce a network address, the host WRITE adds the relative **SCRAMNet+** address and virtual page offset.

network address = relative address + virtual page offset

For example: network address = 12340 + 400000 = 412340

This network address is then transmitted to all of the **SCRAMNet+** nodes and is written to that address. In nodes where the address does not exist in **SCRAMNet+** memory, the WRITE is ignored.

The example in Figure 4-1 shows the memory-sharing relationships between various nodes in the virtual-paging mode. Node 1 shares data with nodes 3, 4, 8, and 9. Node 2 shares data with nodes 5, 6, 7, and 9. Node 8 shares data with nodes 1,3, and 9. Node 7 shares data with nodes 2, 5, and 9. Node 9 shares data with all nodes.

5.2.2 Memory Considerations

When using **SCRAMNet+** shared-memory, consider the following:

PROGRAM AND DATA LIMITATIONS

Limitations on application program size and variable data size for a host computer system also apply to applications which use **SCRAMNet+** memory because it becomes part of the host system.

DATA CACHING

The ability for a computer to write a copy of data to a local fast memory for quicker access later must be turned off during a **SCRAMNet+** memory read. Since other nodes may be changing the data, it is critical that the processor read the data directly from **SCRAMNet+** memory. This is processor dependent and does not always apply.

MEMORY MAPPING

SCRAMNet+ memory is mapped by all operating systems in constant-length blocks called memory pages.

NOTE: To ensure that a compiler or operating system does not try to use unused portions of **SCRAMNet+** memory to store other program segments, the **SCRAMNet+** memory common blocks should be declared to be sized to an integer multiple of the processor memory page size. If this is not done, most compilers will try to optimize memory usage by filling out the **SCRAMNet+** memory pages with other data. This can cause random results when this local data is transmitted around the network.

5.2.3 Control/Status Registers

The **SCRAMNet+** boards are controlled through CSRs for node status, setting interrupt vectors, setting interrupt locations, receiving interrupt addresses, mode control and other functions. These registers may be accessed by linking to the I/O page and reading from or writing to the registers as if they were memory. The method used to access the registers depends on the particular computer and operating system being used.

These registers are set only during the **SCRAMNet+** Network initialization. Once the control portion of the CSR is set up for the desired mode operation, the node functions as transparent shared memory and references to the CSRs are not required. However, the status portions of the registers will need to be accessed for interrupt servicing and for checking for error conditions. Section 5.0 CSR DESCRIPTIONS discusses the definition and use of each bit in the CSRs. Appendix A contains a list of the CSRs and a brief identification of each bit.

5.3 Initialization

The initialization of the **SCRAMNet+** node from a cold boot is determined by the settings of the EEPROM (see Section 3.0 INSTALLATION).

No fiber-optic cable connections are required to perform a READ/WRITE to the local host's **SCRAMNet+** memory, The control registers CSR0 and CSR2 should both be zero at this point and **SCRAMNet+** memory is available for access. The memory address will remain at '0' and be disabled until programmed with the EEPROM Initialization Program.

☞ **NOTE**: All **SCRAMNet+** nodes in the fiber-optic network ring must be powered on unless they have a Fiber Optic Bypass Switch or Quad Switch installed.

5.4 Basic Send/Receive Configuration

The minimum configuration which allows basic send and receive operation is accomplished without interrupts.

- Set CSR0 to ‘F000’ *hex* to insert the node and initiate the reset of the FIFOs.
- Set CSR0 to ‘8003’ *hex* to insert the node, toggle the reset of the FIFOs and enable network activity.
- Set CSR2 to ‘C040’ *hex* to use BURST mode and disable Fiber-optic Loopback mode.
- READ CSR1 to read-out any latched error conditions.
- READ CSR1 again to check for any existing error conditions.
- Check for carrier detect fail (this means there are fiber-optic cabling problems from the transmitter of the node downstream).
- WRITE a value to memory from at least one node. This will enable all powered node transmitters and check for fiber-optic ring integrity.
- READ CSR1 to check for any error conditions.

5.5 Network Ring

Data is passed from one node to the next by fiber-optic or coaxial cable. Given a three node network configuration with nodes A, B and C, the following connections would be made:

- The transmitter pair from node A is connected by fiber-optic cable to the receiver pair of the next node B.
- The transmitter pair from node B is connected by fiber-optic cable to the receiver pair of node C.
- The transmitter pair of node C is then connected to the receiver pair of node A, thus completing a fiber-optic network ring.

5.5.1 Message Contents

The smallest **SCRAMNet+** Network message packet consists of 82 bits. This basic message format contains five fields: Source ID, Age, Control, Data Address, and Data Value. The message can be described as follows:

Table 5-7 SCRAMNet+ Message Contents

START	ID	AGE	CONTROL	DATA ADDRESS	DATA VALUE
1	8+P	8+P	1 1 1 RES INT RTY	5+P 8+P 8+P	8+P 8+P 8+P 8+P

For every 8 bits of data in the message there is a parity bit attached.

SOURCE ID

This 8-bit field contains the node ID of the originating node. Value ranges from 0 to 255, so there can be 256 nodes on the network ring.

AGE

This 8-bit field increments by one as a message passes through each network node. If the age ever exceeds 256 (the maximum number of nodes on the network), the message is removed from the network.

CONTROL BITS

RES - Reserved.
INT - When this bit is set it signals an Interrupt Message.
RTY - Retry message used only in error-correction mode (PLATINUM.)

DATA ADDRESS

This 21-bit (A[22:2]) field contains the relative **SCRAMNet+** memory address. Bits A0 and A1 are always zero for a longword boundary.

DATA VALUE

This 32-bit field contains the data value in **SCRAMNet+** memory that is currently being updated around the ring. When the PLUS mode is enabled, data size may vary up to 256 bytes or 1024 bytes depending on the option selected.

5.5.2 Protocol

BURST MODE

BURST Mode is the normal protocol for **SCRAMNet+**. The BURST mode is enabled by setting CSR2[12] OFF, and CSR2[15,14] ON. The BURST mode protocol allows each node to continuously transmit messages onto the network ring. This mode uses a 4-byte fixed-length message packet for data transfer.

PLATINUM MODE

The PLATINUM mode is BURST mode with error correction enabled. PLATINUM mode is enabled by setting CSR2[12] OFF; CSR2[14] ON; and CSR2[15] OFF See the **SCRAMNet+** Protocol Mode Definition table on page 5-9.

PLUS MODES

The PLUS mode allows variable-length message packets in which sequentially addressed data in the Transmit FIFO is transferred as a block in a single packet.

Enable BURST PLUS by setting CSR2[15], CSR2[14], and CSR2[12] ON, and selecting the desired maximum message packet size by setting CSR2[11] to ‘1’ for 1024 bytes, or ‘0’ for 256 bytes. Both BURST modes are open loop, non-error-corrected modes of operation.

Enable PLATINUM PLUS by setting CSR2[15] OFF, CSR2[14,12] ON, and selecting the desired maximum message packet size by setting CSR2[11] to ‘1’ for 1024 bytes, or ‘0’ for 256 bytes.

The node appends 4-byte data values with sequential addresses until the maximum of 256 or 1024 bytes is reached, a non-sequential address is detected, the Transmit FIFO is empty, or a transmit interrupt event is detected. In both BURST and PLATINUM modes, the node is permitted to have multiple packets on the ring simultaneously.

The transmission of a PLUS mode message is an automatic function, and for the most part, cannot be controlled. If the appropriate PLUS mode bits are set in the control registers, then the following algorithm applies:

1. If Transmit FIFO is empty, end transmission.
1. If the address field is not equal to the address of the previous transmission + 4, end transmission.
1. If length limit overflow for PLUS mode operation occurs, end transmission.
1. ELSE transmit the four data bytes and when done GOTO step 1.

To maintain a PLUS mode transmission, step 1 requires that new data is written to the **SCRAMNet+** board at a rate greater than or equal to 16.7 MB/sec; this is a 32-bit WRITE every 240 ns. Any delay in the host data WRITE will result in failure of step 1, and a premature end to the PLUS mode transmission.

While this method results in the reliable generation of a PLUS mode transmission, it increases the node latency. The **SCRAMNet+** device automatically increases PLUS mode throughput (when blocking is not used) when needed due to high-throughput host, very busy network, etc.

ERROR CORRECTION

Error correction is the automatic retransmission of a **SCRAMNet** Network message when the original message is received in error by the originating node. The message will be retransmitted indefinitely until it is received correctly. During Transmit Retry, the same message is being sent. This prevents any new messages from being transmitted by this node. The Transmit FIFO will hold these new messages until the retry message is received correctly.

If the original message is received by the originating node with some type of bit error, then this results in the Transmit Retry bit in CSR1 being set. If the original message is not received by the originating node in the time-out period specified in CSR5, then this results in the Transmit Retry Time-out bit in CSR1 being set. The time-out period is based on the number of nodes in the network ring and the total length of cable used as discussed in paragraph 3.10.4.

5.5.3 Performance

NODE LATENCY

Node latency is an important factor in networked application in real-time systems design. Data transfer around the network, while fast, does have a measurable delay.

Node latency can be defined as the time delay at a node before a foreign message can be retransmitted. This delay is a minimum of 247 ns; the time to transmit one byte. The maximum node latency depends on the maximum message size and could be from 800 ns to 61.8 µs, depending on the message length selection. To approximate the total maximum delay on the network, multiply the maximum node latency by the number of nodes in the system, and add a propagation delay of 5 ns/meter multiplied by the total message path of the ring in meters.

DATA TRANSFER

While the **SCRAMNet+** Network appears as a shared-memory system, it is still a data network. The **SCRAMNet+** Network includes a series of FIFO buffers to collect data changes until they are transmitted to the other nodes. The Transmit FIFO and the Interrupt FIFO are both 1024 messages in length. These numbers may become significant when performing data transfers of large blocks of data in a short period of time.

HOLDOFF MODE

If the Transmit FIFO becomes full, subsequent READ or WRITE cycles to **SCRAMNet+** memory will be extended until the Transmit FIFO is no longer full (see paragraph 5.11.3 for more information).

SHARED-MEMORY WRITE

SCRAMNet+ shared-memory is based upon a 32-bit word. If an 8- or 16-bit WRITE occurs from the host system, then the 32-bit word that contains that 8- or 16-bit WRITE is sent on the network. Therefore, it is important that other nodes do not simultaneously modify other 8- or 16-bit segments within that 32-bit word.

5.5.4 Throughput

A maximum throughput of 6.5 MB/sec could be achieved if only one node were transmitting data, assuming the host CPU could offer the data at that rate. When more than one node is transmitting in BURST mode, then the effective output per node is 6.5 MB/sec divided by the number of transmitting nodes. In BURST and BURST PLUS modes, the node never retransmits its own messages.

In the BURST PLUS mode, a 256-byte packet provides 16.2 MB/s of data throughput. A 1024-byte packet provides 16.7 MB/s maximum data throughput.

When multiple nodes are transmitting in the BURST mode, the network data passing through the other nodes can affect that node’s output performance. If a node’s receiver is so busy that the Transceiver FIFO is never empty, and the node has already sent a message, then the node will have to wait before it can send another message of its own until either one of its messages comes back or the timer runs out. When the node’s own message is received, it is not placed in the Transceiver FIFO thereby creating an opportunity for the node to send a message from the Transmit FIFO.

In PLATINUM and PLATINUM PLUS modes, error detection is enabled. This will affect node latency in that some messages must be retransmitted.

NETWORK TIME-OUT

Reset the transmit time-out according to the mode of operation selected by writing a 16-bit non-zero value to CSR5 as described in paragraph 3.10.4.

5.6 Auxiliary Control RAM

The ACR is an 8-bit register. However, only ACR[4:0] are implemented. ACR[7:5] are not defined.

Table 5-8 ACR Functions

Bit	Function
0	Receive Interrupt Enable (RIE)
1	Transmit Interrupt Enable (TIE)
2	External Trigger 1
3	External Trigger 2
4	HIPRO Location Enable
7-5	Reserved

When ACR Enable CSR0[4] is set, shared memory is not accessible by the host, and the ACR byte is viewed as the least significant byte of every shared-memory four-byte address. The ACR byte value controls the external trigger and/or interrupt action(s) taken whenever a WRITE occurs to any byte of the shared-memory 4-byte word. Table 5-8 describes the ACR functions.

If these ACR actions are disabled, then no action will be taken when an interrupt condition exists unless override bits in CSR0 or CSR8 are set.

The external trigger and/or interrupt action and/or HIPRO mode for a particular shared-memory location is defined by setting these bits. Once the ACR has been defined, set ACR Enable CSR0[4] back to zero so that shared-memory can again be accessed. The ACR actions are still in effect, but the ACR bytes can no longer be accessed while the ACR Enable bit is zero.

In order for the ACR values to take effect for interrupt action, the following **SCRAMNet+** CSR actions should be considered for the type of interrupt operation desired:

- Host Interrupt Enable to receive network interrupts
- Network Interrupt Enable to transmit network interrupts
- Interrupt on Memory Mask Match Enable for interrupts from memory WRITEs

The five bits of the ACR can be to achieve varied results for any shared-memory location.

NOTE: Shared-memory locations cannot be used as HIPRO and interrupt locations simultaneously.

In order for the external triggers 1 and 2 to take place, ACR[2] and ACR[3], respectively, must be set. In order for the HIPRO mode to become active, ACR[4] must be set for those selected memory addresses where this is to occur. Additionally, CSR2[13] must be set to enable the HIPRO mode.

Receive and/or Transmit (CSR0[1:0]) must be enabled in order for the node to receive and/or transmit network data. There are other combinations of CSR settings to achieve varied interrupt results. Section 5.0 CSR DESCRIPTIONS describes the **SCRAMNet+** CSRs in detail.

5.7 Interrupt Controls

SCRAMNet+ allows a processor to receive interrupts from and/or transmit interrupts to any other processors on the network, including the originating processor. Table 5-9 indicates the various sources for interrupt control.

5.7.1 Interrupt Options

Table 5-9 Interrupt Controls

CONDITION	REGISTER	DESCRIPTION
Host Interrupt Enable	CSR0[3]	Must be set in order to receive any interrupts from the network.
Receive Interrupt Enable (RIE)	ACR[0]	Generates an interrupt to the host from network data received at the associated shared-memory location.
Transmit Interrupt Enable (TIE)	ACR[1]	Generates an interrupt message to the network for a host WRITE to the associated shared-memory location.
Interrupt on Memory Mask Match Enable	CSR0[5]	Permits a shared-memory interrupt. Must be set in order to receive any interrupts from the network
Override RIE	CSR0[6]	Generates an interrupt to the host regardless of the ACR RIE setting upon receipt of any network interrupt message.
Enable Interrupt on Error	CSR0[7]	Generates an interrupt request as specified in the CSR9 Mask register as the corresponding bit in CSR1 is set..
Network Interrupt Enable	CSR0[8]	Permits transmission of interrupt data to the network.
Override TIE	CSR0[9]	Transmits message Interrupt to the network regardless of the ACR TIE setting.
Reset Interrupt FIFO	CSR0[13]	Toggle from ‘0’ to ‘1’ to ‘0’ to reset Interrupt FIFO.
Interrupts Armed	CSR1[14]	During the interrupt operation indicates conditions to receive interrupt are active. If ‘0’, no interrupts will be received by the host. Any WRITE to CSR1 will reset to ‘1’.
Enable Interrupt on Own Slot	CSR2[10]	In conjunction with CSR2[9] enables host self-interrupt.
LSP of Interrupt Address	CSR4[15:0]	Interrupt Address A15 - A0.
MSP of Interrupt Address	CSR5[6:0]	Interrupt Address A22 - A16. Works in conjunction with CSR4[15:0].
Interrupt FIFO Not Empty	CSR5[15]	When ‘0’, Interrupt FIFO is empty. If ‘1’, CSR5 and CSR4 contain legitimate interrupt address(es).
Receive Interrupt Override	CSR8[10]	When set, all incoming network messages are treated as interrupt messages.
Interrupt on Error Mask	CSR9[15:0]	Interrupts for specified error/status conditions .

SEND/RECEIVE WITH INTERRUPTS

- Set CSR0 to ‘0010’ *hex* to enable the Auxiliary Control RAM (ACR).
- Clear the **SCRAMNet+** ACR by writing zeros to the entire address range.
- Set the **SCRAMNet+** ACR memory locations which are to receive and/or transmit interrupts.
- Reset CSR0 to disable the ACR.
- Set CSR0 to ‘F000’ *hex* to insert the node and initiate the reset of the FIFOs.
- Set CSR0 to ‘8003’ *hex* to insert the node, toggle the reset of the FIFOs and enable network activity.
- Set CSR2 to ‘C040’ *hex* to use BURST mode and disable Fiber-optic Loopback mode.
- READ CSR1 to read-out any latched error conditions.
- READ CSR1 again to check for any existing error conditions.
- Check for carrier detect fail (this means there are fiber-optic cabling problems from the transmitter of the node downstream).
- WRITE a non-interrupt value to memory from at least one node. This will enable all powered node transmitters and check for fiber-optic ring integrity.
- READ CSR1 to check for any error conditions.
- Put the interrupt service routine (ISR) in place.
- Set CSR0 to ‘812B’ *hex* to enable receive and transmit interrupts.
- Set CSR0 to ‘81AB’ *hex* to enable Interrupt On Errors.

5.8 Interrupt Conditions

Interrupts are generated under two different conditions:

- A **SCRAMNet+** network data WRITE to shared-memory
- A **SCRAMNet+** network error/status detected on the local node

5.8.1 Network Data WRITE

As indicated in Figure 5-2, Transmit Enable CSR0[1] must be set before any message can be sent. Only those nodes which have Transmit Interrupt Enable ACR[1] set for selected addresses send an interrupt bit out with the data packet on the network. Only those nodes which have Receive Interrupt Enable ACR[0] set for that address will generate an interrupt signal to their host processor.

The host issues a WRITE to **SCRAMNet+** shared memory. If Override TIE CSR0[9] or ACR TIE ACR[1] is set and Network Interrupt Enable CSR0[8] is set, then the interrupt message is transmitted (INT = 1). Otherwise, the message is transmitted without the interrupt bit set (INT = 0). (See Table 5-7, page 5-4)

Network data WRITE interrupts can be accomplished by two methods:

- **Forced**. Any data WRITEs to any shared memory from the network will generate an interrupt.
- **Masked or Selected**. Data writes to selected shared-memory locations from the network. Under either of these two methods, an interrupt can be generated and received by the same host processor if desired. This condition is termed as “Self-Interrupt”.

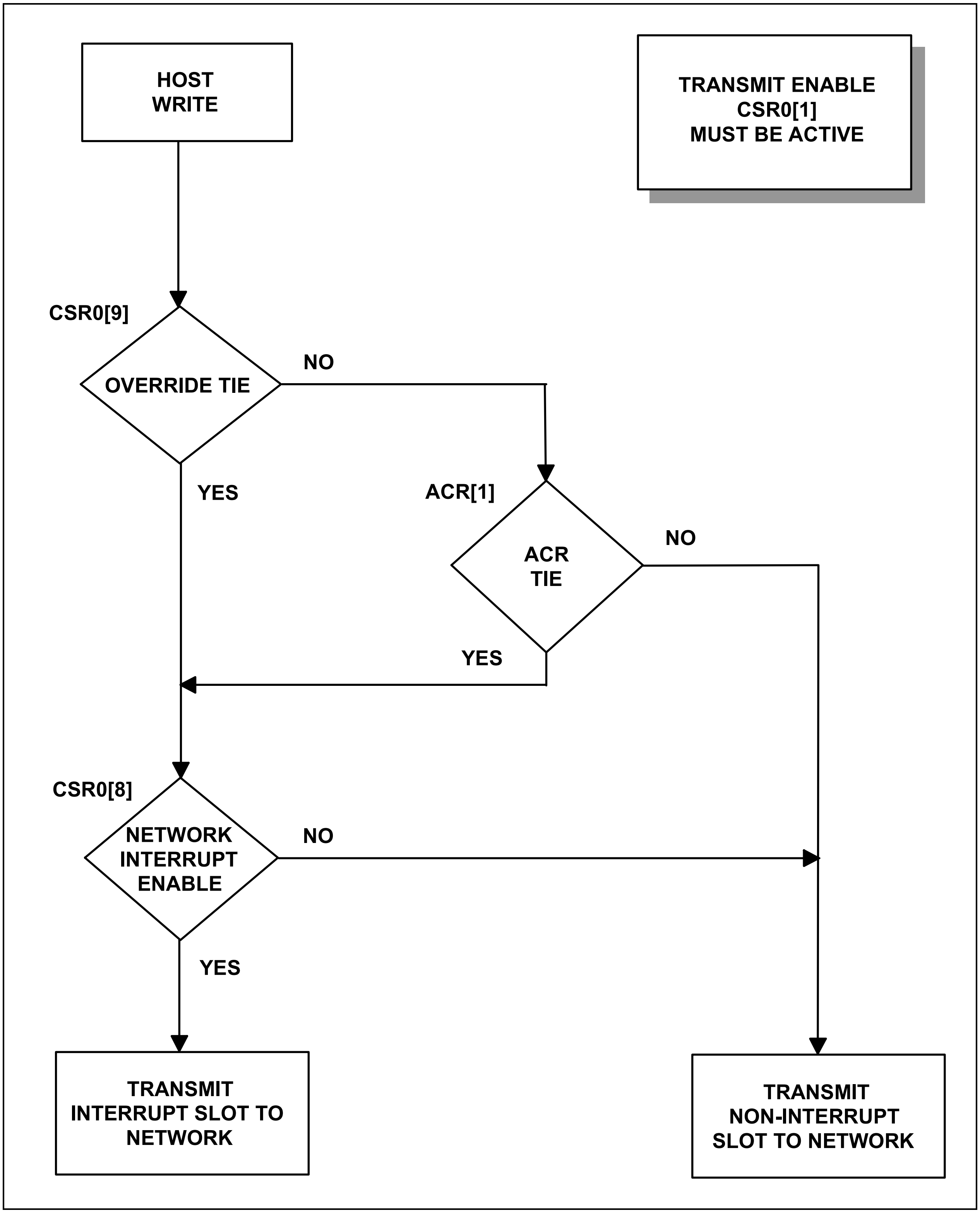

HOST WRITE
TRANSMIT ENABLE CSR0[1] MUST BE ACTIVE
CSR0[9]
OVERRIDE TIE
NO
YES
ACR[1]
ACR TIE
NO
YES
CSR0[8]
NETWORK INTERRUPT ENABLE
NO
YES
TRANSMIT INTERRUPT SLOT TO NETWORK
TRANSMIT NON-INTERRUPT SLOT TO NETWORK

Figure 5-2 Transmit Interrupt Logic

FORCED INTERRUPT

The forced-interrupt method works the same as the selected-interrupt method with the exception of choice of interrupt locations. All shared-memory locations are automatically set up to receive and/or transmit interrupts depending upon the override bits set in CSR0 or CSR8.

MASKED OR SELECTED INTERRUPT

The masked- or selected-interrupt method requires choosing **SCRAMNet+** shared-memory locations on each node to receive and/or transmit interrupts. These shared-memory locations may also be used to generate signals to external triggers. The procedure for selecting shared-memory locations for interrupts and/or external triggers is explained in paragraph 5.6: Auxiliary Control RAM.

CSR5 contains the Interrupt FIFO Not Empty bit CSR5[15].

SELF-INTERRUPTS

Set CSR2[10:9] to enable self-interrupts. This allows the message with the interrupt bit set to be processed as an incoming network interrupt. CSR2[9] enables the node's own message to be received as a network message. CSR2[10] allows the interrupt bit to generate an interrupt if it is set.

Receive Interrupt logic is described in Figure 5-3. If a native message is received and Write Own Slot CSR2[9] is enabled, and Enable Interrupt on Receipt in own Slot CSR2[10] is set, the logic then checks for Receive Interrupt Enable. If Override RIE CSR0[6] is set or ACR RIE ACR[0] is set, and if Interrupt Mask Match Enable CSR0[5] is set, the address is placed on the Interrupt FIFO.

☞ **NOTE**: Interrupt data is not filtered when the data filter is enabled

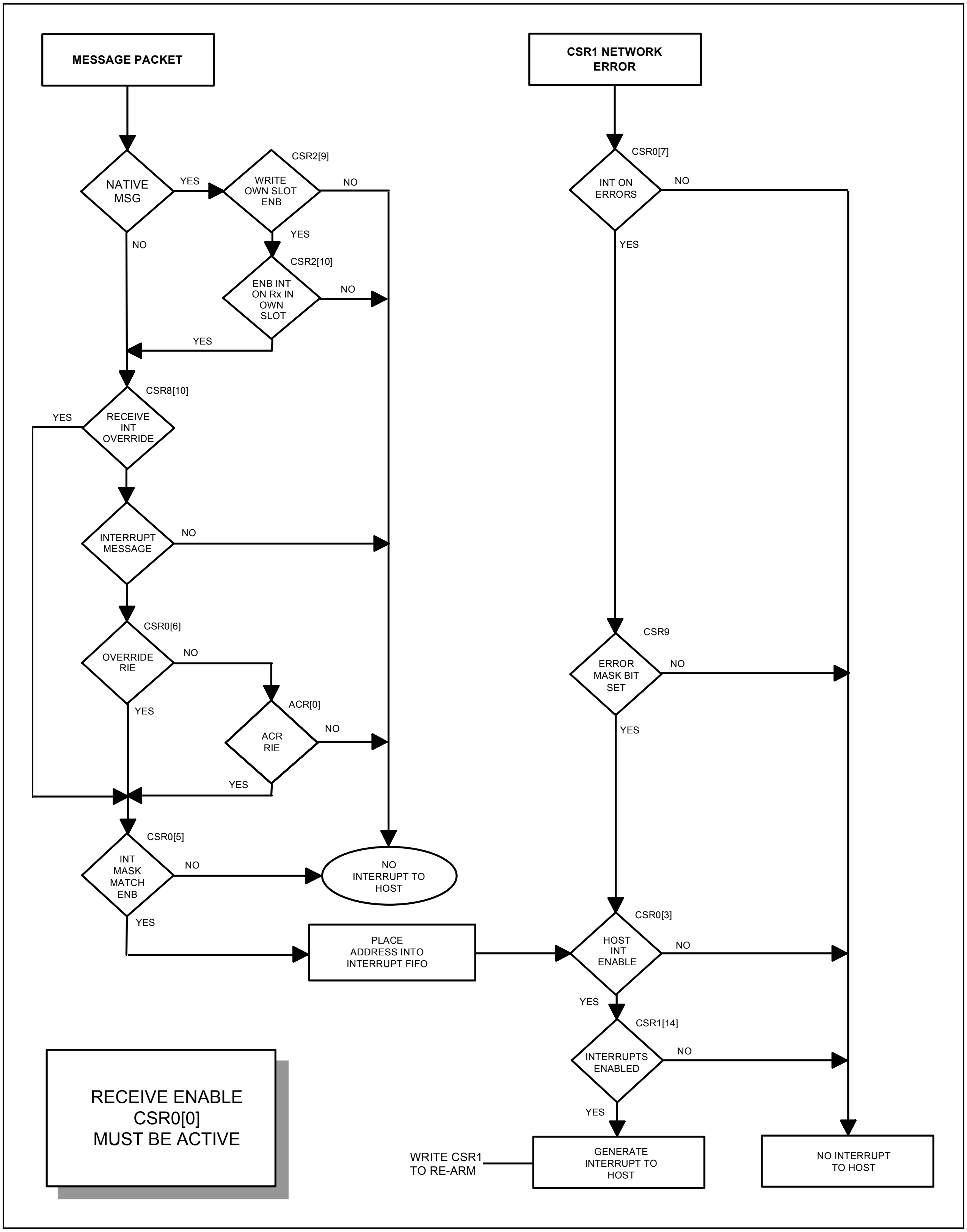


Figure 5-3 Receive Interrupt Logic

5.8.2 Network Error

The second interrupt condition is designed to intercept network errors. CSR1 contains the following error conditions which may be masked by CSR9:

Table 5-10 Interrupt Error/Status Conditions

Bit	Interrupt
0	Transmit FIFO Full
1	Transmit FIFO Not Empty
2	Transmit FIFO 🏳 Full
3	(Not masked for errors)
4	Interrupt FIFO Full
5	Protocol Violation
6	Carrier Detect Failure
7	Bad Message
8	Receiver Overflow
9	Transmit Retry
10	Transmit Retry Time-out
11	Redundant Rx/Tx Fault
12	General Purpose Counter/Timer
13	(Not masked for errors)
14	(Not masked for errors)
15	Fiber Optic Bypass Not Connected

Each of these conditions is identified by the corresponding bit being set (value 1) in CSR1. If any of the preceding conditions are set and the Interrupt On Memory Mask Match Enable CSR0[5] is set, then an interrupt will be generated to the host computer. Additional information about each error condition is contained in Section 5, Table 5-2: CSR1.

If a Network Error is received (Figure 5-3), and if Interrupt on Error CSR0[7] and Host Interrupt Enable CSR0[3] are set, and Interrupts are Enabled CSR1[14], then the message generates an interrupt to the host. If additional network data interrupts occur before the processor is able to service the interrupt, those shared-memory locations are updated and the addresses are added to the Interrupt FIFO queue. However, no additional interrupt signals are sent to the host until interrupts are armed by writing to CSR1.

5.8.3 Interrupt Handling

The Interrupt FIFO is accessed via CSR4 and CSR5. CSR5 contains the most significant seven bits of the 23-bit **SCRAMNet+** interrupt address and CSR4 contains the remaining 16 bits of the interrupt address. (The 23-bit address allows for future expansion of memory.) CSR5 also contains Interrupt FIFO Not Empty (bit 15).

NOTE: The **SCRAMNet+** Network has a longword (32-bit) oriented shared memory. External Triggers and Interrupts will occur when any of the four bytes associated with a longword are accessed. The Interrupt FIFO contains the longword address. If each of the four bytes of an interrupt location are written into as byte accesses, then four interrupts to the same longword address will be generated. Likewise, if each word of an interrupt location is written into as 16-bit shortwords, then two interrupts to the same longword address will be generated.

The two values of CSR5 and CSR4 make up the interrupt address. When an interrupt is received, the ISR should READ CSR5 first in order to check the Interrupt FIFO Not Empty bit. If this bit is set (value is ‘1’), then READ CSR4. If this bit is CLEAR (value is 0) then the Interrupt FIFO is empty. Therefore, the interrupt was due to an error, assuming that Enable Interrupt On Error is set.

Every READ from CSR5 and CSR4 will contain the **SCRAMNet+** memory address of the data received from the network interrupt. Every READ of CSR5 and CSR4 will automatically increment the FIFO pointer to the next interrupt address for both registers. CSR4 should be read only if Interrupt FIFO Not Empty CSR5[15] is set. Continue to READ CSR5 and CSR4 until the Interrupt FIFO Not Empty bit is zero. Writing any value to CSR1 will re-enable interrupts. See Page 5-28 for an example of a standard ISR algorithm for handling interrupts from the **SCRAMNet+** boards.

WARNING: If HIPRO is enabled, an interrupt may affect the sequence of addresses on a READ/WRITE if **SCRAMNet+** is manipulated in the ISR.

If an interrupt occurs before the interrupts have been armed, the interrupt will be placed in the Interrupt FIFO and it will occur when the interrupts are armed (CSR 1).

5.9 External Triggers

Two external triggers are provided by the **SCRAMNet+** Network. The external triggers will occur only if the ACR has been configured to enable them. Triggers 1 and 2 are generated by **SCRAMNet+** shared-memory access. Triggers generate a 26.64 ns TTL level compatible, non-terminated, output.

- Trigger 1 - Host READ/WRITE: ACR[2] enables
- Trigger 2 - Network WRITE: ACR[3] enables

Trigger 1 will be generated for any host access to **SCRAMNet+** memory.
Trigger 2 will be generated by a network WRITE to the **SCRAMNet+** memory.

The trigger-output signals are available through the external-trigger-connection pins, if installed on the board. Also, pin 7 of the Auxiliary Connector is connected to TRIG1.

The triggers can be used to measure time intervals or to start or stop an external event

EXAMPLE 1 - MEASURE TRANSACTION TIME

Select a shared-memory address in node A and enable trigger 1 by setting ACR[2]. Select the same memory address in node B and enable trigger 2 by setting ACR[3]. Connect a wire from TRIG1 to an oscilloscope. Connect a wire from TRIG2 to the oscilloscope. Initiate a HOST WRITE to the node A memory address. When the corresponding NETWORK WRITE occurs, the time difference can be measured.

EXAMPLE 2 - MEASURE RING TIME

Enable WRITE-ME-LAST mode on node A. Select a shared-memory address and enable trigger 1 and trigger 2 for that address. Connect a wire from TRIG (pin 3 - trigger 1 OR 2) to an oscilloscope. Initiate a HOST WRITE to that memory address. The time difference displayed on the oscilloscope will approximate the ring time—the time it takes from the HOST WRITE on node A to the NETWORK WRITE on node A.

EXAMPLE 3 - SET OFF AN ALARM

Enable trigger 1 for the shared-memory address of a critical datum by setting ACR[2]. Connect a wire from TRIG1 to an alarm light. When the HOST WRITE to that memory address occurs, the light will come on.

5.10 General Purpose Counter/Timer

This 16-bit counter/timer can be programmed by changing CSR9[13] and CSR9[14] to select the desired mode as described in Table 5-11. CSR8[9] can be set to override the counter/timer mode settings and allow the counter/timer to run free at 26.66 ns (37.5 MHz). CSR9[12] can be set to generate an interrupt upon overflow of the counter/timer. The output from the event counter/timer is stored in CSR13. See Section 5, page 5-7, 5-13, and 5-16 for more information.

5.10.1 Available Modes

The General Purpose Counter/Timer register (CSR13) can be used as a counter or a timer. The mode is selected via a combination of registers and bits which are explained on page 5-13. Table 5-11 describes the counter/timer modes available:

Table 5-11 General Purpose Counter/Timer Modes

Mode	Description
Count Errors:	Each error detected in CSR1 will increment the counter by 1.
Count Trigger 1 and 2:	Each time a trigger event occurs the counter will increment.
Transit Time:	Set this mode and clear the counter. The counter will begin counting when the next message is transmitted, and stop counting when any message generated by this node is received.
Network Events:	Count incoming network messages.
Free Run @ 26.66 ns:	Increment counter using internal 37.5 MHz clock. Counter will roll over every 1.78 ms.
Free Run @ 1.706 µs with Trigger 2 to CLEAR:	Increment counter using the 585.9 KHz clock. Counter will roll over every 111.8 ms. Assertion of Trigger 2 will clear the counter.

5.10.2 Rollover/Reset

A rollover/reset can generate an interrupt if selected to do so from the Interrupt On General Purpose Counter/Timer Overflow Mask CSR9[12]. When this bit is set, whenever the counter register (CSR 13) rolls over or overflows, an interrupt is generated to the host system. Interrupt-on-errors mode CSR0[7] must be enabled in order for this to work properly. The counter/timer will roll over when it reaches 65,536.

Only one mode may be selected at a time since they use the same counter/timer register (CSR13) for output.

5.10.3 Presetting Values

The counter/timer register counts upward and may be preset with a value to arrive at the desired interrupt interval.

EXAMPLE:

To set an interrupt to occur every 100 ms, the counter register is preloaded with ‘8717’, so that when the counter reaches 65,536, only 100 ms would have passed instead of 111.8 ms.

The value of ‘8717’ was determined by dividing the desired interrupt time of 100 ms (100,000 μs) by the increment frequency of 1.760 μs which results in 56,818. This is the number that would be in the counter register after 100 ms. To obtain a starting value of ‘8717’, subtract 56,818 from 65535. The counter/timer will not roll over until it reaches 65,535 + 1.

See section 5.0, pages 5-7, 5-13, and 5-15 for additional information.

5.11 Modes of Operation

5.11.1 Data Filter

Many implementations of shared-memory tend to rewrite data values to memory which have not actually changed. In order to reduce network traffic, the **SCRAMNet+** board has the ability to compare the new value with the old value of data and avoid sending unchanged data values out on the network. This feature is a type of data filtering and can be enabled without affecting node latency while improving network throughput. See Figure 5-4.

CSR0[10] and CSR0[11] control the operation of data filtering as shown in Table 5-12 (see Section 5.0 for details of CSR operation):

- CSR0[10] enables the data filtering during transmission to the **SCRAMNet+** memory and only for the address space above the first 4 K bytes.
- CSR0[11] enables the address space of the first 4 K bytes to be data-filtered in conjunction with CSR0[10].

Table 5-12 Data Filter Options

CSR0[11]	CSR0[10]*	Result
0	1	Only the address space above 4 K bytes of shared memory is data-filtered
1	1	All shared memory is data-filtered

* CSR0[10] must be ON for any data filtering to take place on that node.

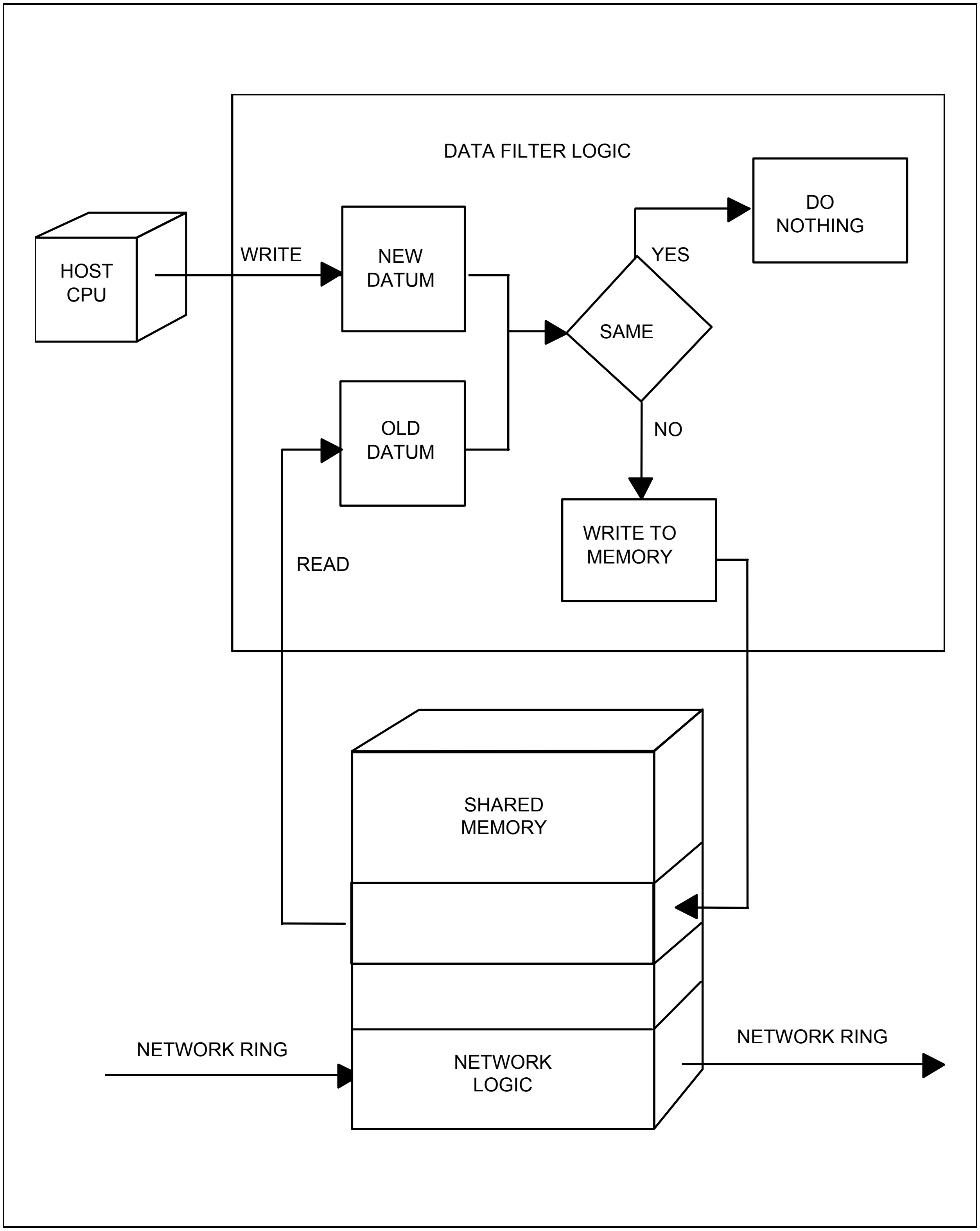


Figure 5-4 Data Filter Logic

5.11.2 HIPRO Mode

WRITE

The **SCRAMNet+** network message is based on 32-bit longword data. If a host processor is only capable of 8- or 16-bit data transactions, then the **SCRAMNet+** bandwidth is quartered or halved, respectively. For each 32-bit data transaction from the host, two 16-bit data transactions, or four 8-bit transactions will occur on the bus each requiring a **SCRAMNet+** network WRITE.

The **HIPRO** mode was created to provide an efficient means to transmit two 16-bit data transactions as one 32-bit network WRITE. The first of the two 16-bit WRITEs will be to memory but will be prevented from going onto the network. The second 16-bit WRITE to memory will trigger the WRITE of the 32-bit location to the network. HIPRO WRITE will not work if Disable Host to Memory Write CSR2[8] is set, because the first 16-bit WRITE must be to the **SCRAMNet+** memory.

NOTE: The order of writing the shortwords or bytes into the longword boundary does not matter. However, it is important that a HIPRO location does receive a second shortword WRITE if a first shortword WRITE is initiated, or a total of 4-byte WRITEs if a byte WRITE is initiated, to a HIPRO location. Otherwise, it is possible to partially WRITE a 32-bit location causing the data to be lost and never be transmitted.

The **HIPRO** mode is also effective for transmitting user defined 16-bit data items. Two 16-bit data items may be sent as one 32-bit data item if they are consecutive and lie within the same 32-bit address boundary.

HIPRO mode is selected for those memory addresses which have ACR[4] set. **HIPRO** Enable CSR2[13] must also be set. A non-HIPRO location WRITE should be used to synchronize the HIPRO flags.

5.11.3 Loopback Modes

Each node has a Monitor and Bypass mode, Wire Loopback mode, Mechanical Switch Loopback mode, and a Fiber-optic Loopback mode. These modes are used to check the node’s performance and to test transmit/receive circuitry. The loopback mode routes data which would normally be transmitted on to the network, directly back to the node from different points.

Table 5-13 depicts the data path for the Monitor and Bypass mode.

Table 5-14 depicts the data path for Wire Loopback Mode.

Table 5-15 depicts the data path for Mechanical Switch Loopback Mode.

Table 5-16 depicts the data path for the Fiber-optic Loopback Mode.

Table 5-17 depicts the data path for the Insert Mode.

MONITOR AND BYPASS MODE

This mode permits the node to receive data only. Network data is not re-transmitted.

Table 5-13 Monitor and Bypass Mode States

State	Register	Setting
Receive Enable	CSR0[0]	ON
Transmit Enable	CSR0[1]	DON’T CARE
Insert Enable	CSR0[15]	OFF
Enable Wire Loopback	CSR2[7]	OFF

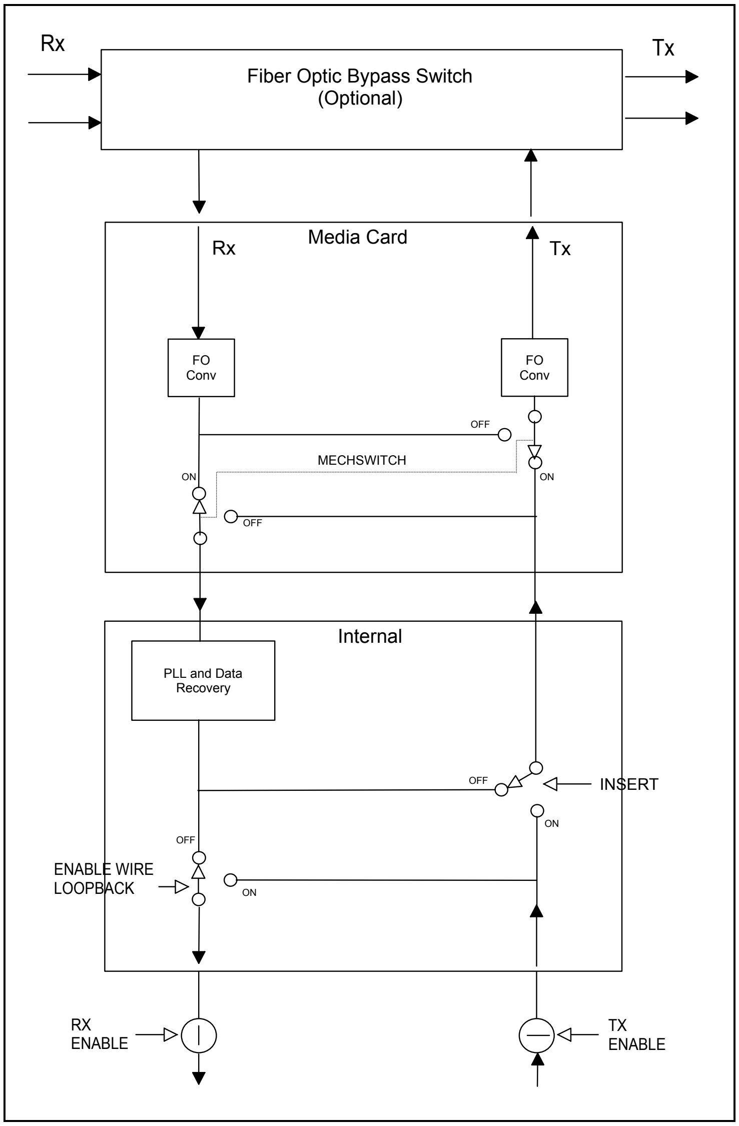


Figure 5-5 Monitor and Bypass Mode

WIRE LOOPBACK MODE

The Wire loopback permits testing of the internal circuitry and needs no manual external modifications to work. In this mode, the transmitted signal does not leave the board.

Table 5-14 Wire Loopback Mode States

State	Register	Setting
Receive Enable	CSR0[0]	ON
Transmit Enable	CSR0[1]	ON
Insert Enable	CSR0[15]	OFF
Enable Wire Loopback	CSR2[7]	ON

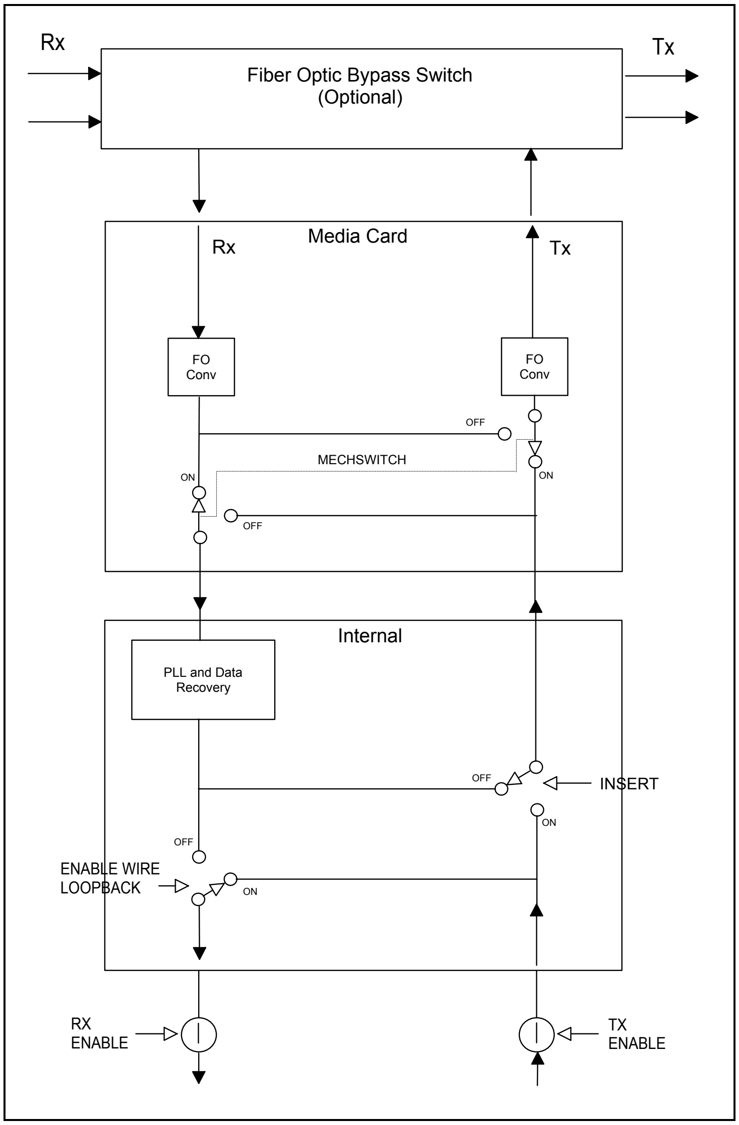


Figure 5-6 Wire Loopback Mode

MECHANICAL SWITCH LOOPBACK MODE

This mode permits testing of all circuitry up to and including a major portion of the Media Card.

Table 5-15 Mechanical Switch Loopback Mode States

State	Register	Setting
Receive Enable	CSR0[0]	ON
Transmit Enable	CSR0[1]	ON
Insert Enable	CSR0[15]	ON
Enable Wire Loopback	CSR2[7]	OFF
Mechanical Switch Override	CSR8[11]	OFF

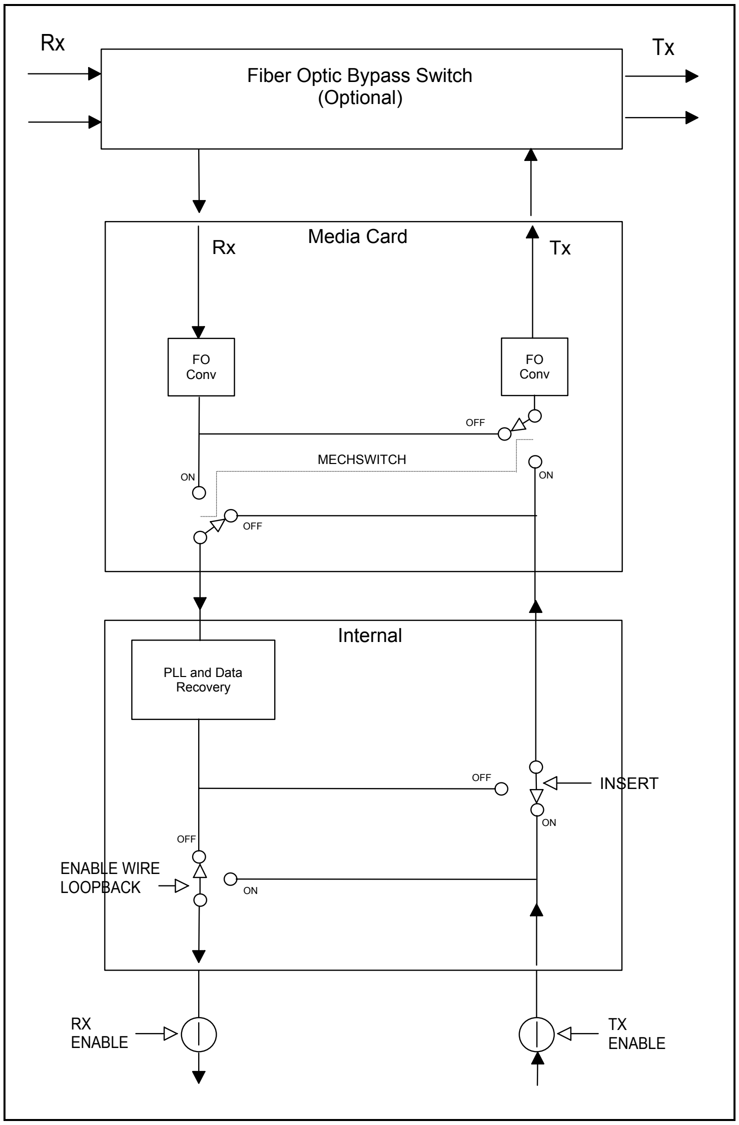


Figure 5-7 Mechanical Switch Loopback Mode

FIBER-OPTIC LOOPBACK

When this mode is invoked, the output of the transmitter is connected by fiber optics directly to the input of the receiver, and the receiver is disconnected from the network.

Table 5-16 Fiber-optic Loopback Mode States

State	Register	Setting
Receive Enable	CSR0[0]	ON
Transmit Enable	CSR0[1]	ON
Insert Enable	CSR0[15]	ON
Enable Wire Loopback	CSR2[7]	OFF
Disable Fiber-optic Loopback	CSR2[6]	OFF
Mechanical Switch Override	CSR8[11]	ON

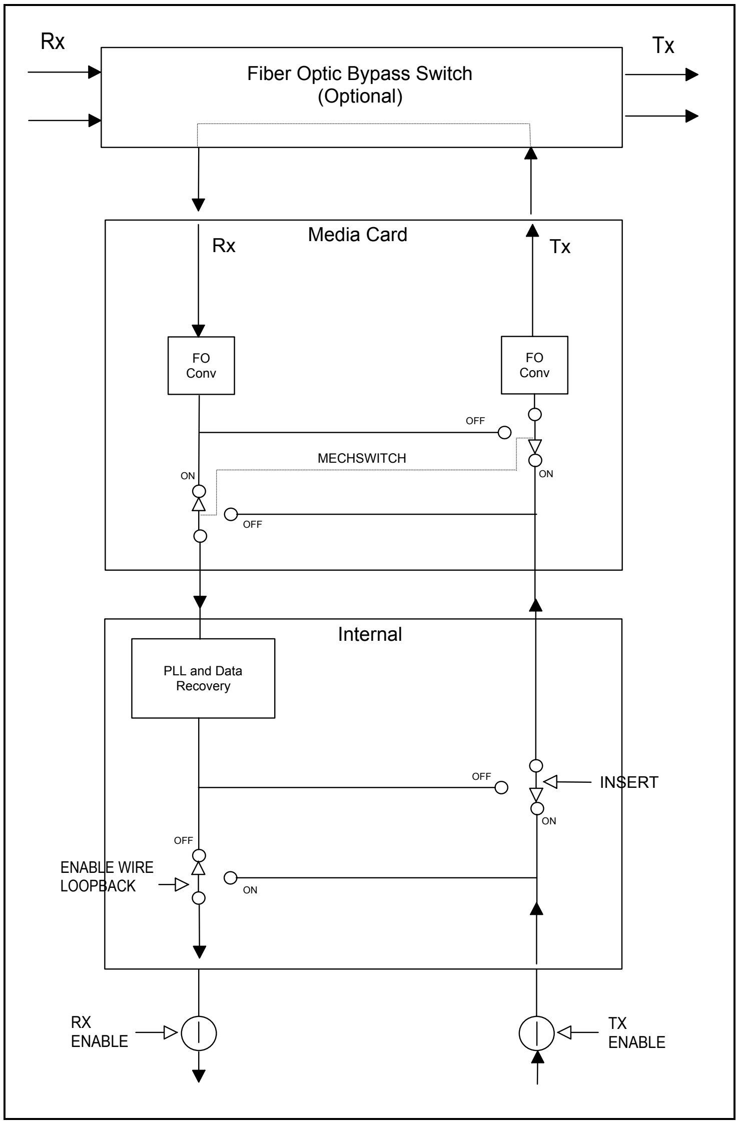


Figure 5-8 Fiber-optic Loopback Mode

The optional Fiber Optic Bypass Switch must be installed for this to work. However, in the absence of the Fiber Optic Bypass Switch, fiber-optic cables could be run from the node's transmitter output connectors to the receiver input connectors. This configuration, with Insert Node enabled, would constitute a Fiber-optic Loopback mode for stand-alone testing. Disable Fiber-optic Loopback CSR2[6] must be set ON when the node is in use as a part of the network. However, this configuration could not be used in a network ring in the place of an Fiber Optic Bypass Switch because it would cause a break in ring continuity.

The Fiber Optic Bypass Switch is used to provide fiber-optic ring continuity when a node is powered down or in loopback mode. CSR2[6] controls the operation of the Fiber Optic Bypass Switch by enabling or disabling Loopback mode. To disable the Fiber-optic Loopback mode, set CSR2[6] ON. This state allows data to be transmitted and received on the network ring for this node.

When the Fiber-optic Loopback mode is enabled (CSR2[6] OFF), the Fiber Optic Bypass Switch does not allow network data to be received by the node. Likewise, no data can be transmitted by the node into the network ring.

When power is lost to the Fiber Optic Bypass Switch, Fiber-optic Loopback mode is enabled regardless of its prior state in order to maintain ring integrity. This is also the default power-up state.

NODE INSERT MODE

In this mode the node becomes part of the network (Figure 5-9).

Table 5-17 Node Insert Mode

State	Register	Setting
Receive Enable	CSR0[0]	ON
Transmit Enable	CSR0[1]	ON
Insert Node	CSR0[15]	ON
Enable Wire Loopback	CSR2[7]	OFF
Disable Fiber-optic Loopback	CSR2[6]	ON
Mechanical Switch Override	CSR8[11]	ON

NOTE: Do not enable the Wire Loopback and Fiber-optic Loopback and/or Mechanical Switch loopback modes simultaneously. A node in Wire Loopback mode and Insert Node will create a break in the network ring which will disable all nodes.

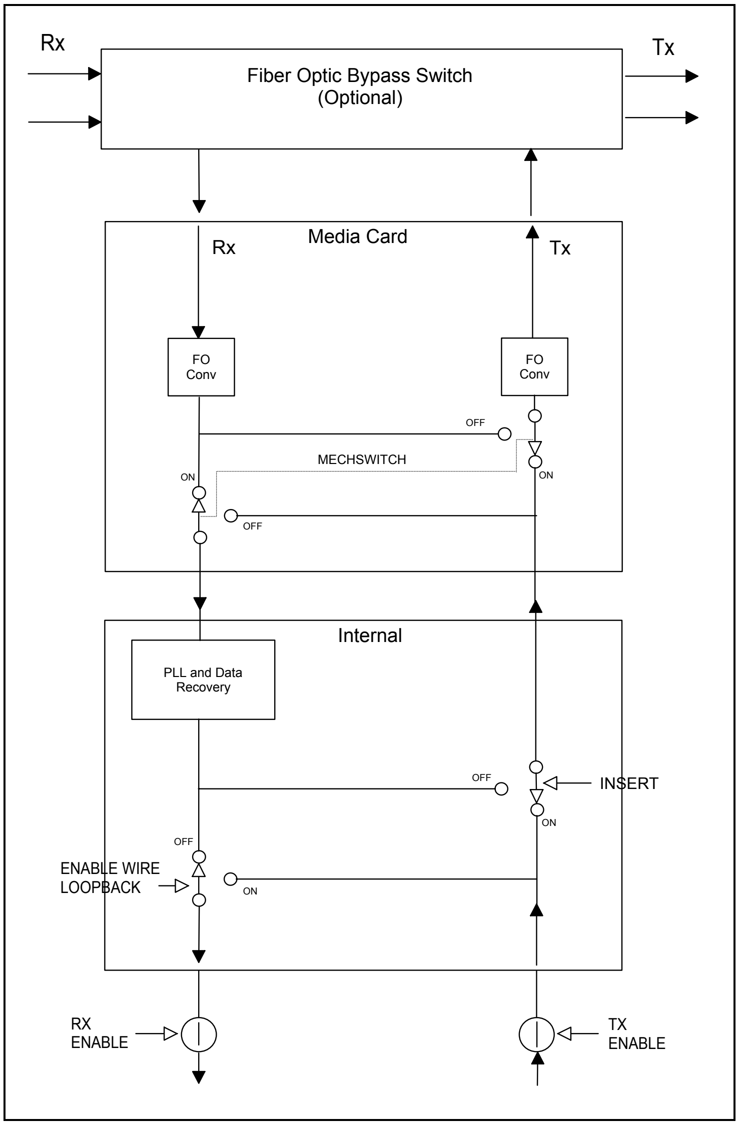


Figure 5-9 Insert Mode

5.11.4 Holdoff Mode

To enable Holdoff mode, set CSR8[1] OFF. Holdoff mode automatically slows down CPU data WRITEs to the **SCRAMNet+** memory when the Transmit FIFO becomes full. The Transmit FIFO serves as a buffer between the **SCRAMNet+** memory and the **SCRAMNet+** network.

The Transmit FIFO can become full when the host CPU is writing to **SCRAMNet**+ memory faster than the network can absorb the data. If a CPU is capable of writing to the **SCRAMNet**+ memory on the bus at such a rate that the Transmit FIFO becomes full (1024 deep), data could be lost.

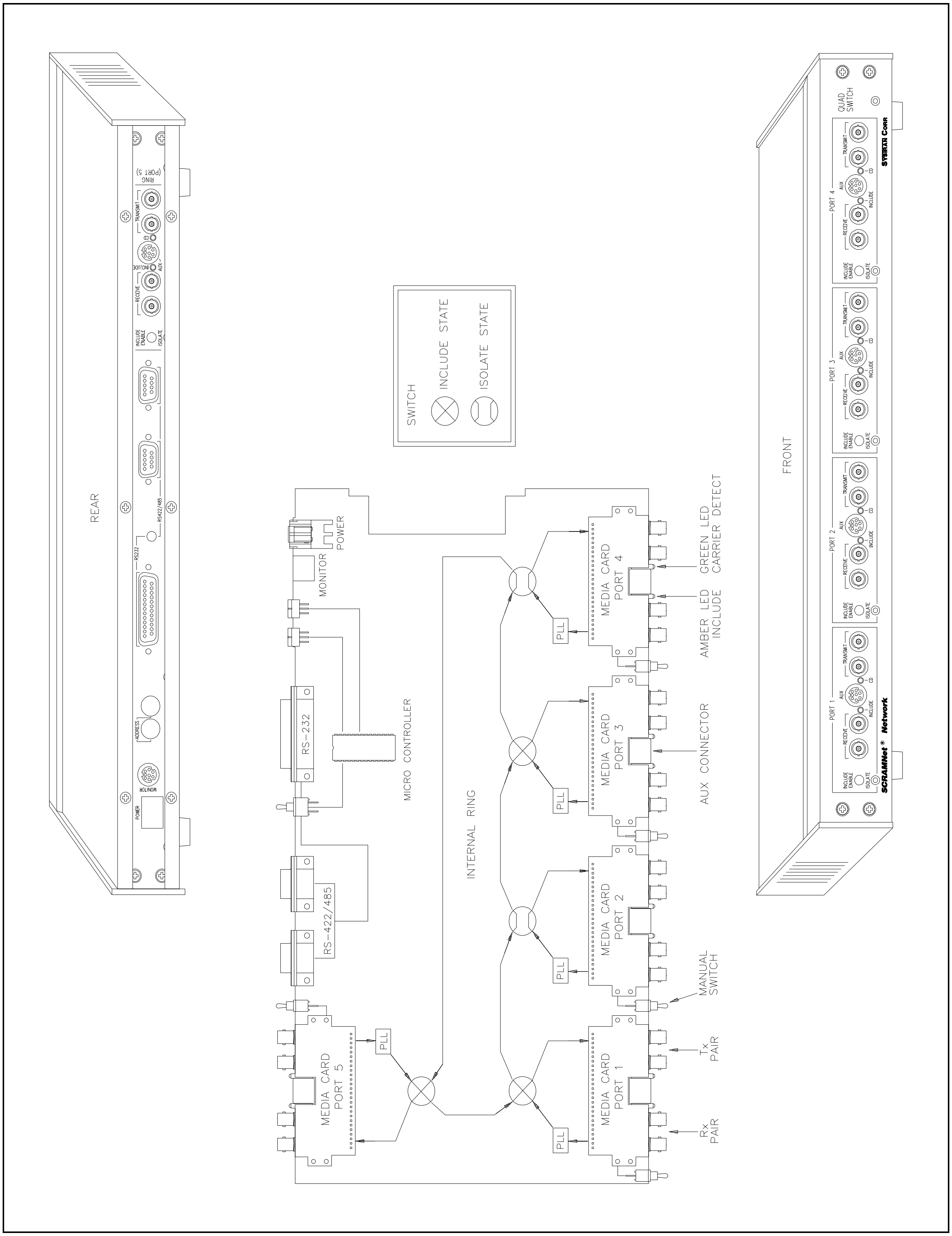


Figure 5-10 Quad Switch

In the event that the Transmit FIFO becomes full, the hardware will automatically extend the next WRITE cycle until the Transmit FIFO empties at least one message. This prevents the loss of any data and is transparent to the user.

5.11.5 Write-Me-Last Mode

The Write-Me-Last mode of operation allows the originating node to be the last node in the ring to have the data deposited to its memory. When the host performs a WRITE to the **SCRAMNet+** shared-memory, it is not immediately written to the host memory, but is first sent to the other **SCRAMNet+** nodes on the network.

Set CSR2[8] and CSR2[9] to enable the Write-Me-Last mode. If desired, this mode can also be used to generate interrupts to the originating node by setting CSR2[10] as well. CSR2[8] is the Disable Host to Shared Memory Write.

5.12 Quad Switch

The Quad Switch is a switching center and is used to dynamically configure active **SCRAMNet** and **SCRAMNet+** ring(s).

The Quad Switch provides dynamic configuration of up to five separate rings. Each separate ring is connected to a port on the Quad Switch. Refer to Figure 5-10. Each ring can be isolated from the other rings or can be included with one or more of the other attached rings.

There is a single logical ring internal to the Quad Switch. The Quad Switch has five external ports which allow access to this logical ring. Ports 1 through 4 are accessible on the front of the Quad Switch cabinet. Port 5 access is at the rear of the cabinet.

All five ports have standard **SCRAMNet** transmitters and receivers. Each port can transmit data to and receive data from the internal ring.

The Quad Switch is designed so that a port will be switched into the ring if all its switching controls are enabled. Any one of the switching controls can cause the port to be switched out.

CSR0[3] HIE and CSR0[5] IMME must be set in order to set up interrupts.
CSR1[15:0] contain various error and status conditions. Interrupts are re-armed whenever any value is written to CSR1.

CSR4[15:0] contain the interrupt address bits A0-A15.

CSR5[6:0] contain the interrupt address bits A22-A16.
CSR5[15] contains the Interrupt FIFO Not Empty status.

If an interrupt has been received by the host processor from the SCRAMNet+ Network interrupt logic, the Interrupt Service Routine will be invoked. Interrupts will be disabled until re-armed by writing to CSR1. Until that time, all other interrupts will be written into the Interrupt FIFO where they can be processed in the Interrupt Service Routine.

If CSR0[7] Interrupt on Errors is enabled, and the Interrupt FIFO is empty on the initial check of CSR5 in the Interrupt Service Routine, then an interrupt due to an error has occurred.

```
Read CSR5
        Test the Interrupt FIFO Not Empty status bit 15
        If (Interrupt FIFO is Empty)
                Read CSR1 to determine the error condition(s)
                Respond to any error conditions
        End if

        While (Interrupt FIFO is NOT Empty)
                Save interrupt address bits A22-A16 from CSR5 (from previous read)
                Read CSR4 and save interrupt address bits A15-A0
                                        • • •
                Service interrupt according to interrupt address data or address
                                        • • •
                Read CSR5 and save Interrupt FIFO Empty status
        Endwhile

     Write to the system motherboard Programmable Interrupt Controller (PIC) at the address
     dictated by the Interrupt Level selected to re-arm interrupts:
        0x20  = 0x20  (Interrupt Level 1-8)
        0xA0 = 0x20  (Interrupt Level 9-15)

        Write to CSR1 to re-arm interrupts
        Return from interrupt service routine
```

Figure 5-11 Interrupt Service Routine

6.0 CSR DESCRIPTIONS

6.1 Description

This section describes each Control/Status Register and the function of each bit. The name of each bit is indicative of its set state.

The registers are described using bit 0 as the Least Significant Bit (LSB). For example: Inserting A7C3 *hex* in a 16-bit register would set bits 0, 1, 6, 7, 8, 9, 10, 13, and 15 ON.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	1	1	1	1	1	0	0	0	0	1	1
A				7				C				3			

TABLE OF CONTENTS

Table 5-1 CSR0

Bits	General SCRAMNet+ Enable and Reset (READ/WRITE)
1-0	**Network Communications Mode** - Bit 0 controls the receive enable, and Bit 1 controls the transmit enable.
	00 **None** - In this mode, all communications between the node shared memory and the network is inhibited. The node is still able to pass network traffic but does not receive or transmit any data. Loopback modes are also meaningless unless the Host to Shared Memory WRITE bit is enabled.
	01 **Receive Only** - In this mode, any received message is processed and written to node shared memory. Data written by the host is placed in the node shared memory and in the Transmit FIFO but is not sent out on the network. In this mode, the Transmit FIFO will fill and if the Error Interrupt is enabled, Transmit FIFO Full interrupt will be triggered. Before changing modes from Receive-Only to either Transmit-Only or Transmit/Receive, the Transmit FIFO should be cleared. If not, all buffered transmit messages will be sent out on the network.
	10 **Transmit Only** - In this mode, any received message bypasses the shared memory and is passed on. Any message written by the host to node shared memory is transmitted on the network. However, any received message is not written to node shared memory. (Transmissions are subject to data filter characteristics.)
	11 **Transmit/Receive** - In this mode, any received message is processed, written to node shared memory and passed on. Any message written by the host to node shared memory is transmitted on the network. This is the normal operation. (Transmissions are subject to data filter characteristics.)
2	**Redundant Transceiver Toggle** - When this bit is cycled ‘0’, ‘1’, ‘0’, the optional redundant transceiver selected link is changed.
3	**Host Interrupt Enable** - When this bit is set, a received message that is written to node shared memory as an interrupt will generate an interrupt request, and the address will be written to the Interrupt FIFO. This bit must be set in order to receive any interrupts from the network.

Table 5-1 CSR0 (Continued)

Bits	General SCRAMNet+ Enable and Reset (READ/WRITE)
4	**Auxiliary Control RAM Enable** - When this bit is set, the ACR bytes are swapped in place of the corresponding least-significant byte of every four-byte word in **SCRAMNet+** memory. The values written to those ACR byte locations dictate the type of interrupt that will occur when the 4-byte memory location is written into. The ACR has five bits for interrupt control:
	ACR[0] - **Receive Interrupt Enable** - Setting this bit generates an interrupt to the host for network interrupt data received in this location.
	ACR[1] - **Transmit Interrupt Enable** - Setting this bit generates an interrupt to the network for a host WRITE to this shared memory location.
	ACR[2] - **External Trigger 1** - Setting this bit generates a trigger signal to an external connector whenever there is a host READ/WRITE access to this shared memory location.
	ACR[3] - **External Trigger 2** - Setting this bit generates a trigger signal to an external connector whenever there is a network WRITE to this shared memory location.
	ACR[4] - **HIPRO location enable** - Setting this bit causes the two 16-bit data or four 8-bit items within the 32-bit address boundary to be transmitted as one 32-bit network message. CSR2[13] must also be set for this action to occur.
5	**Interrupt On Memory Mask Match Enable** - This bit must be set in order for any type of memory interrupt to occur.
6	**Override Receive Interrupt Enable Flag** - When this bit is set, an interrupt is generated to the host by any interrupt data received from the network regardless of the status of the ACR Receive Interrupt bit.
7	**Enable Interrupt on Error** - When this bit is set, Interrupt FIFO Full, Protocol Violation, Bad Message and/or Receiver Overflow conditions cause an interrupt request.
8	**Network Interrupt Enable** - This bit must be set to transmit interrupt data to the network.
9	**Override Transmit Interrupt Enable Flag** - When this bit is set, an interrupt is sent out on the network regardless of the status of the ACR Transmit Interrupt bit.

Table 5-1 CSR0 (Continued)

Bits	General SCRAMNet+ Enable and Reset (READ/WRITE)
10	**Enable Transmit Data Filter** - When clear, the entire address space is not filtered and the node is capable of transmitting all messages written to the node shared memory by the host on the network. When set, the data-filter function is enabled for the address space above the first 4 K bytes of **SCRAMNet+** memory. Bit 11 controls the lower 4 K bytes.
11	**Enable Lower 4 K Bytes For Data Filter** - When set, the lower 4 K bytes of address space is data filtered if bit 10 is also set. When disabled, the address space will not be filtered.
12	**Reset Receive/Transmit FIFO** - This bit must be toggled from zero to one and back to zero in order to reset the Receive/Transmit FIFO. The R/T FIFO is a temporary high-speed holding area for data flowing through the network. **NOTE**: If the R/T FIFO were to be reset during active network transmissions, the data in the FIFO at that time would be lost and it would cause errors on the downstream nodes in the network ring.
13	**Reset Interrupt FIFO** - This bit must be toggled from ‘0’ to ‘1’ and back to ‘0’ to reset the Interrupt FIFO.
14	**Reset Transmit FIFO** - This bit must be toggled from ‘0’ to ‘1’ and back to ‘0’ to reset the Transmit FIFO.
15	**Insert Node** - This bit controls the nodes communications mode on the network as either a receiver only or a receiver/transmitter. On power-up, this bit is OFF which translates to the receiver-only mode. This allows user-written software (on each host processor on the network) to be initiated from one node whenever the network is started cold. When this bit is ON, the node is “inserted” into the network ring as a receiver/transmitter which is the normal operating mode if the Fiber-optic Loopback CSR2[6] is disabled. This bit is invalid when the Enable Wire Loopback CSR2[7] is ON.

Table 5-2 CSR1

Bits	**Error Indicators** (READ Only with WRITE/RESET for interrupts) Reading CSR1 resets the latched error conditions by clearing bits 0,2,4,5,6,7,8,9,10,11,12,13.
0	**Transmit FIFO Full (Latched)** - When this bit is set, the Transmit FIFO Full condition exists. This occurs when there is more data coming from the host to the network than the network can absorb. When the shared memory is full, host WRITEs are held off by the **SCRAMNet+** host interface logic until the Transmit FIFO is no longer full.
1	**Transmit FIFO Not Empty** - This bit does not represent any type of error condition, but rather just a report on the state of the Transmit FIFO. A ‘0’ represents an empty FIFO, where a ‘1’ indicates at least one message in the FIFO.
2	**Transmit FIFO 7/8 Full (Latched)** - This bit indicates that the Transmit FIFO is 7/8 full. A ‘0’ represents a FIFO that is less than 7/8 full, where a ‘1’ indicates the FIFO is backing up and is more than 7/8 full.
3	Always 0
4	**Interrupt FIFO Full (Latched)** - When this bit is set, the Interrupt FIFO Full error condition exists. Reset the Interrupt FIFO by toggling CSR0[13] to ON then to OFF.
5	**Protocol Violation (Latched)** - When this bit is ON, there has been a signal error at the physical layer (fiber or coax) resulting from noise on the transmission lines or a result of hardware failure. It can be any one of the following: Missing transition for two clock periods on either line Parity error Framing error
6	**Carrier Detect (Latched)** - This bit is set if the receivers do not detect any or enough output from the previous node’s transmitters. This is usually an indication that the fiber-optic lines have become disconnected or there may be dust/dirt where the fiber-optic connections have been made. Visually inspect the network lines.
7	**Bad Message (Latched)** - When this bit is set, the hardware has detected an error in the message packet received on the network. If this error persists, it is an indication that a hardware problem on the **SCRAMNet+** board may exist.
8	**Receiver Overflow (Latched)** - When this bit is set, the Receive FIFO has received more data than the node is able to process. This condition may indicate a hardware problem on the board.
9	**Transmit Retry (Latched)** - This bit is set if a message returns to the originating node with bit errors. The message is automatically retransmitted indefinitely until it returns without bit errors. This is considered to be an error condition.
10	**Transmit Retry Time-out (Latched)** - This bit is set if a message does not return to the originating node within the time-out value specified in CSR5. The message is automatically retransmitted indefinitely until it returns. This is considered to be an error condition.

Table 5-2 CSR1 (continued)

Bits	Error Indicators (READ Only with WRITE/RESET for interrupts)
11	**Redundant Transmit/Receive Fault (Latched)** - This bit is set if the currently selected optional redundant transceiver has faulted and reverted to the other link. The default value is ‘0’
12	**General Purpose Counter/Timer Overflow (Latched)** - This bit toggles a 16-bit counter/timer. The events to be counted/timed are set using CSR8[9]; CSR9[13]; and CSR9[14]. The output is held in CSR13. The counter/timer can: count errors, count trigger events for triggers 1 and 2, transmit time, network events, free run @ 26.66 ns, and free run @ 1.706 ns with trigger 2 CLEAR.
13	**Current Link (Latched)** - This bit tells which of the optional redundant transceivers is currently selected as the active link. The default value is ‘1’ = A.
14	**Interrupts Armed** - During interrupt operation, this bit indicates that the conditions to receive an interrupt are active. If this bit is ‘0’, then no interrupts will be received by the host. When CSR1 is written to, then the interrupts-armed bit returns to an active status.
15	**Fiber Optic Bypass Not Connected** - This is a status bit concerning the installation of the optional Fiber Optic Bypass Switch. A ‘0’ in this bit indicates that the bypass switch is installed while a ‘1’ indicates it is not installed. Fiber-optic Loopback CSR2[6] mode is dependent upon the Fiber Optic Bypass Switch being installed.

Table 5-3 CSR2	
Bits	**Node Control (READ/WRITE)**
5-0	These bits are related to lines connected through the MUX control port and are available to the host interface. They are not required to connect to anything
6	**Disable Fiber-optic Loopback** - When this bit is '0' (power up default), the output of the transmitter is connected by fiber optics directly to the input of the receiver, and the receiver is disconnected from the network. The optional Fiber Optic Bypass Switch must be installed for this mode to be effective. This mode is valid only when the Insert Node CSR0[15] is ON. Set this bit to disable the loopback mode when the node is in use as a part of the network.
7	**Enable Wire Loopback** - When this bit is set, the output of the transmitter is connected by wire directly to the input of the receiver, and the receiver is disconnected from the network. The purpose of this bit is purely diagnostic. This mode is valid only when the Insert Node CSR0[15] is OFF.
8	**Disable Host to Memory Write** - When this bit is set, the host WRITEs are not written to the host node's shared memory, but are sent out on the network if Transmit CSR0[1] is ON.
9	**Write Own Slot Enable** - When this bit is set, the message slot (or packet) sent out to the network can be received by the originating node. This is not the normal procedure but may be used (in conjunction with CSR2[10] when it is desired to generate an interrupt to the host, written by the host.
10	**Enable Interrupt On Own Slot** - When this bit is set, a message with the interrupt bit set can be received by the originating node if CSR2[9], is also set. This coupling enables a host processor to interrupt itself (Self Interrupt).
11	**Message Length Limit** - Variable maximum message size: 1024 bytes or 256 byte. It is used in conjunction with CSR2[15], CSR2[14] and CSR2[12] to enable Plus mode communication protocols.

Write-Me-Last/Self-Interrupt Mode Definition

Bit 10	Bit 9	Bit 8	Mode
0	1	1	WRITE ME LAST mode
1	1	0	SELF-INTERRUPT mode
1	1	1	WRITE ME LAST with SELF-INTERRUPT mode

Table 5-3 CSR2 (continued)	
Bits	**Node Control (READ/WRITE)**
12	**Variable Length Messages on Network** - When ON, this bit enables variable length messages. It is used in conjunction with CSR2[15], CSR2[14] and CSR2[11] to enable PLUS mode communication protocols (see below).
13	**HIPRO Enable** - When this bit is set, the two 16-bit shortwords associated with the longword addressed at ACR[4], will be transmitted onto the network as one 32-bit longword. The first shortword WRITE will be held until the second shortword WRITE occurs, which results in the 32-bit data value to be written to the network. **Exceptions**: HIPRO will not work when Disable Host to Memory WRITE CSR2[8] is set. HIPRO will not work when writing two separate shortwords while using interrupts.
14	**Multiple Messages** - This bit allows multiple native messages on the network. It is used in conjunction with CSR2[15], CSR2[12] and CSR2[11] to enable the BURST mode communication protocol (see below).
15	**No Network Error Correction** - This bit is used in conjunction with CSR2[12] and CSR2[14] to enable communication protocols: BURST or PLATINUM mode and the variable length message PLUS (+) mode (see below).

SCRAMNet+ Protocol Mode Definition

Network Mode	CSR2[15]	CSR2[14]	CSR2[12]	CSR2[11]
	No Error Correction	**Multiple Message**	**Variable Length**	**Message Size Maximum**
BURST	1	1	0	NO MEANING
PLATINUM	0	1	0	NO MEANING
BURST+	1	1	1	1=1024, 0=256
PLATINUM+	0	1	1	1=1024, 0=256

Table 5-4 CSR3

Bits	Node Information (READ ONLY)
7-0	**Node Number Count** - These bits represent the total number of **SCRAMNet+** nodes on the network. This value is dynamically determined by the hardware and ranges from 0 to 255 depending upon the number of nodes actually on the network. **Transmit AGE** - This field is also used to READ/WRITE the T_AGE[7:0] field. This register reflects this field when the ID_MUX bit in CSR8[0] is set.
15-8	**Node Identification Number** - These bits represent the **SCRAMNet+** node identification number. Each node must have a unique identification number from 0 to 255 for each network ring. The NODE ID need not be in sequential order. **Receive ID** - This field is also used to READ/WRITE the RXID[7:0] field. This register reflects this field when the ID_MUX bit in CSR8[0] is set.

Table 5-5 CSR4

Bits	Interrupt Address (LSP) (READ ONLY)
15-0	**LSP of the Interrupt Address** - These bits represent the LSP of the interrupt address (A15 - A0). Bits 0 and 1 are always ‘0’ since the addresses are on four-byte boundaries.

Table 5-6 CSR5

Bits	Interrupt Address and Status (READ ONLY)*
6-0	**MSP of the Interrupt Address** - These seven bits represent the MSP of the interrupt address (A22 - A16). When coupled with CSR4, this address represents the **SCRAMNet**+ memory location of the interrupt.
13-7	Reserved
14	**Retry Interrupt FIFO Bit** - This bit is set when an interrupt message is received that has its message retry bit set. This can be checked in the interrupt service routine to guard against double interrupts from the same message if it happens to be retransmitted.
15	**Interrupt FIFO Not Empty** - When this bit is clear, the Interrupt FIFO is empty. Do not READ CSR4 when this bit is ‘0’. When this bit is set, it signals that CSR5 and CSR4 contain a legitimate interrupt address.

* Writing the Transmit Time-out value to CSR5 stores it in shadow memory. Do not set this value to ‘0’. A value of ‘0’ prevents host-generated data from leaving the Transmit FIFO.

Table 5-7 CSR6

Bits	ISA Transfer Register
1-0	**Transaction Type (R/W):** 00 = Byte Transaction 01 = Shortword Transaction 1X = Longword Transaction
3-2	Reserved
5-4	**Page Configuration (R)**:* 00 = 8 KB 01 = 16 KB 10 = 32 KB 11 = 64 KB
6	**Page Enable (R)** 1 = ON
7	**SIMM Enable (R)**: If the configuration software finds SIMMs installed, this bit is set to ‘1’. If no SIMMs are installed, a ‘0’ selects the 128 KB on-board memory option. and a ‘1’ selects the 4 KB option.
15-8	Reserved

* These bits are only written from the EEPROM during initialization

Table 5-8 CSR7

Bits	Reserved
15-0	Not Used

Table 5-9 CSR8	
Bits	**General SCRAMNet+ Extended Control Register**
0	**ID Multiplex** - When set to ‘1’, CSR3 contains the T_AGE and RXID fields.
1	**Disable Holdoff** - When set, this bit disables the Holdoff mode.
7-2	These bits are used for programming the EEPROM.
8	**CSR Reset** - Setting this bit causes bus errors. On reset, CSRs load from EEPROM.
9	**General Purpose Counter/Timer Free Run** - Setting this bit causes the GPC to free run at a rate of 37.5 MHz (26.66 ns). This counter mode overrides all other counter mode settings.
10	**Receive Interrupt Override** - When this bit is set, all incoming network messages are treated as interrupt messages.
11	**Mechanical Switch Override** - Normally set to ON. When OFF, Mechanical Switch Loopback mode is invoked.
14-12	**Memory Size Configuration** - These bits indicate the memory-size code and are used in conjunction with the memory address stored in CSR10 and 11. The memory size is automatically calculated. (See below)
15	Reserved (Always 1).

Memory Size Configuration

Bit 14	Bit 13	Bit 12	Memory Size
1	1	1	4 KB
1	1	0	128 KB
1	0	1	512 KB
1	0	0	1 MB
0	1	1	2 MB
0	1	0	4 MB
0	0	1	8 MB

Table 5-10 CSR9	
Bits	**SCRAMNet+ Interrupt On-Error Mask***
0	**Transmit FIFO Full Mask**
1	**Transmit FIFO not Empty Mask**
2	**Transmit FIFO 7/8 Full Mask**
3	**Built In Self Test Stream (BIST)** - Internal 82-bit BIST shift register output.
4	**Interrupt FIFO Full Mask**
5	**Protocol Violation Mask**
6	**Carrier Detect Fail Mask**
7	**Bad Message Mask**
8	**Receiver Overflow Mask**
9	**Transmitter Retry Mask**
10	**Transmitter Retry Due to Time Out Mask**
11	**Redundant TX/RX Fault Mask**
12	**Interrupt on General Purpose Counter/Timer Overflow Mask**
13	See Below
14	See Below
15	**Fiber Optic Bypass Switch Not Connected Mask**

General Purpose Counter/Timer Modes

CSR8[9]	CSR9[14]	CSR9[13]	Counter Modes
0	0	0	Count Errors
0	0	1	Count Trigs (1&2)
0	1	0	Transit Time
0	1	1	Network Events
1	1	X	Free Run @ 26.66 ns
1	0	1	1.706 µs w/trig 2 CLR

* To enable an On-Error mask, set the bit to ‘1’.

Table 5-11 CSR10	
Bits	**Reserved**
15-0	Not Used

Table 5-12 CSR11	
Bits	**Reserved**
15-0	Not Used

Table 5-13 CSR12

Bits	SCRAMNet+ Virtual Paging Register	
0	VP	**Virtual Paging Enable**. When ON, this bit enables Virtual Paging.
4-1	-0-	Always zero
5	VP_A12	**Virtual Page number.** The significance of this register is dependent on the memory size. (e.g. For 4 MB, only VP_A22 is valid; for 4 KB, VP_A[22:12] are valid.
6	VP_A13	
7	VP_A14	
8	VP_A15	
9	VP_A16	
10	VP_A17	
11	VP_A18	
12	VP_A19	
13	VP_A20	
14	VP_A21	
15	VP_A22	

Table 5-14 CSR13

Bits	General Purpose Counter/Timer	
0	RD_COUNT[0]	This is a General Purpose Counter/Timer register. It can be used to count trigger 1 and 2 events, count errors, or other events as programmed by CSR9[13] and CSR9[14].
1	RD_COUNT[1]	
2	RD_COUNT[2]	
3	RD_COUNT[3]	
4	RD_COUNT[4]	
5	RD_COUNT[5]	
6	RD_COUNT[6]	
7	RD_COUNT[7]	
8	RD_COUNT[8]	
9	RD_COUNT[9]	
10	RD_COUNT[10]	
11	RD_COUNT[11]	
12	RD_COUNT[12]	
13	RD_COUNT[13]	
14	RD_COUNT[14]	
15	RD_COUNT[15]	

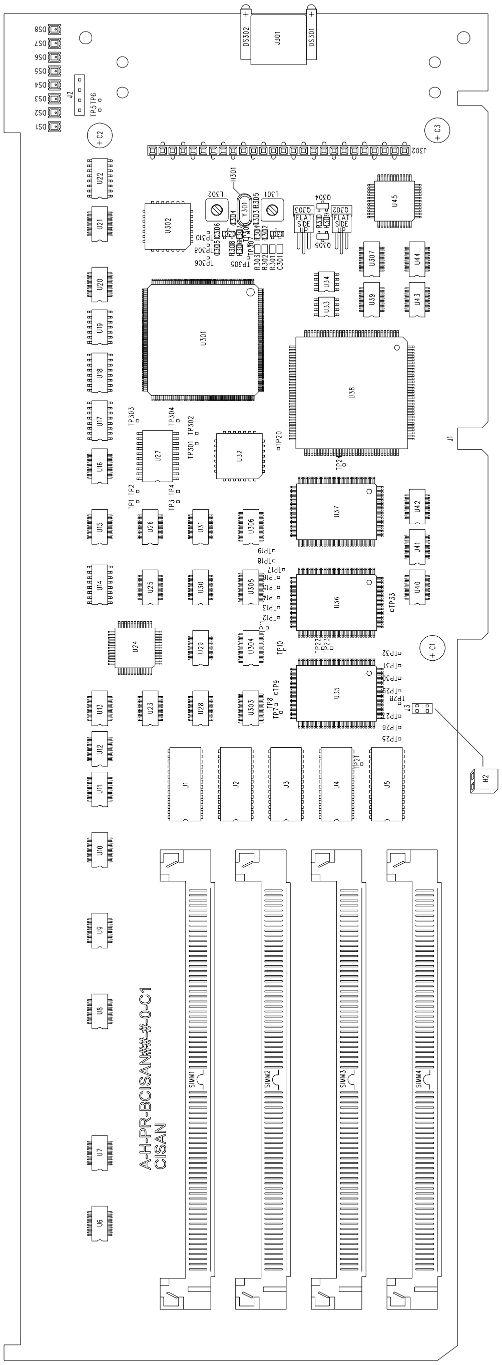
Table 5-15 CSR14	
Bits	**ISA Page Select Register**
0	LSB
1	
2	
3	
4	Page Select Register (R/W)*
5	
6	
7	
8	
9	MSB
15-10	Reserved

* These bits are only used when CSR6 is set

Table 5-16 CSR15	
Bits	**Reserved**
15-0	Not Used

7.0 PHYSICAL FEATURES

7.1 ISA Board Layout



Host and Network Internal Access bi-color LED's

Media Card Connection J302

External Trigger Connections (J2)

ISA Bus Connection (J1)

PnP System Option Jumper (J3)

SIMM Connections

Part Number & Version

Figure 7-1 ISA, Version C1

7.2 ISA Bus Connection (J1)

The board requires a single slot in the computer chassis.

7.3 External Trigger Connections (J2)

The two external triggers will occur only if the ACR has been configured to enable them. Triggers 1 and 2 are generated by **SCRAMNet+** shared-memory access.

7.4 PnP System Option Jumper (J3)

If the host system has a plug-and-play BIOS, it doesn't matter how J3 is set. Activate the board using software by running **scr_cm -activate.**

In non-PnP systems, if J3 is set to "PnP", activate the board using **scr_cm -activate**. If J3 is set to "Non-PnP" the device acts like a normal ISA board, and is active upon boot-up.

7.5 Media Card Connection (J302)

The Media Card is the interface between the **SCRAMNet+** support circuitry and the transmission medium: optical fiber or coaxial cables. It is mounted on the ISA board as a Mezzanine board. The ISA board will support either option, depending on the configuration of your network.

One model of the Media Card has coaxial connections and the other has fiber-optic connections.

The **SCRAMNet+** Support Circuitry supplies the same signal to the Media Card, regardless of the transmission medium supported by the Media Card. The Media Card converts the generic signal from the **SCRAMNet+** Support Circuitry to one appropriate to the transmission medium.

7.6 SIMMs

If there are no SIMMs installed, the shared memory defaults to the 4 KB or 128 KB on-board memory, as ordered from the factory.

SIMMs have the following installation options:

- Low density, 512 KB SIMMs
  1 = 512 KB (SIMM 1)
  2 = 1 MB (SIMM 1 and 2)
  4 = 2 MB (SIMMs 1 through 4)
- High density, 2 MB SIMMs
  1 = 2 MB (SIMM 1)
  2 = 4 MB (SIMM 1 and 2)
  4 = 8 MB (SIMMs 1 through 4)

SIMMs must all be either low density or high density; they can not be mixed. The SIMMs are proprietary and must be ordered from SYSTRAN.

7.7 Part Number and Version

The last two characters of the part number represent the version. For example: A-H-PR-BCISAN##-#-0-C1 indicates the board is version C1.

7.8 Internal Access LEDs

The Host and Network internal access bi-color LED indicators on the board can be used to assist with troubleshooting or fine tuning of the network. There is no external remote indicator, so the chassis must be left open in order to see the LEDs.

The bi-color LEDs show either green (G) or yellow (Y) .

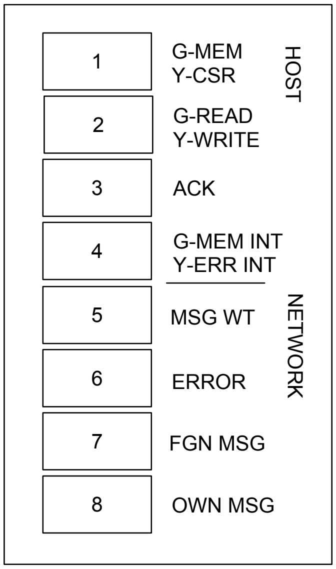


Figure 7-2 LED Indicators

APPENDIX A
CSR SUMMARY

TABLE OF CONTENTS

A.1 CSR0 - General SCRAMNet+ Enable and Reset

Bit	Function	Name
0	Receive Enable	RX_ENB
1	Transmit Enable	TXEN
2	Redundant TxRx Toggle	RTT
3	Host Interrupt Enable	HIE
4	Auxiliary Control RAM Enable	ACRE
5	Interrupt on Memory Mask Match Enable	IMME
6	Override RIE Flag	ORF
7	Interrupt on Errors	IOE
8	Network Interrupt Enable	NIE
9	Override TIE Flag	OTF
10	Enable Tx Data Filter	DFEN
11	Enable Lower 4 Kbytes for Data Filter	EN4K
12	RESET Rx/Tx FIFO	RTRF
13	RESET Interrupt FIFO	RSTIF
14	RESET Transmit FIFO	RTXF
15	Insert Node	INSRT

A.2 CSR1 - Error Indicators

Bit	Function	Name
0	Transmit FIFO Full	TXFF
1	Transmit FIFO Not Empty	TXFNE
2	Transmit FIFO 7/8 Full	TXFAF
3	(Always 0)	Not Used
4	Interrupt FIFO Full	IFF
5	Protocol Violation	PV
6	Carrier Detect Failure	CDF
7	Bad Message	BB
8	Receiver Overflow	RXO
9	Transmit Retry	TXRTY
10	Transmit Retry Time-out	TO
11	Redundant TxRx Fault	RTF
12	General Purpose Counter/Timer Overflow	GPCTO
13	Redundant TxRx Link 1=A/0=B	RTLAB
14	Interrupts Armed - Write to re-arm	IARM
15	Fiber Optic Bypass Not Connected	FOB

A.3 CSR2 - Node Control

Bit	Function	Name
5-0	Available to Host	
6	Disable Fiber Optics Loopback	FO_DIS
7	Enable Wire Loopback	EN_WR_LPB
8	Disable Host to SM Write	DIS_H_M_WR
9	Enable Write of Our Own Slot to Memory	WOSEN
10	Enable Interrupt on Receipt of Own Interrupt Slot	IOSEN
11	1024 vs 256 variable size max (bytes)	LEN_LIMIT
12	Variable length messages on network	VAR_LEN
13	HIPRO Write Enable	HIPRO
14	Allow multiple native messages on network	MULTIPLE_MSG
15	No Network Error Correction	NO_ERR_CRCT

Write-Me-Last/Self-Interrupt Mode Definition

Bit 10	Bit 9	Bit 8	Mode
0	1	1	WRITE ME LAST mode
1	1	0	SELF-INTERRUPT mode
1	1	1	WRITE ME LAST with SELF-INTERRUPT mode

SCRAMNet+ Protocol Mode Definition

Network Mode	CSR2[15]	CSR2[14]	CSR2[12]	CSR2[11]
	No Error Correction	Multiple Message	Variable Length	Message Size Maximum
BURST	1	1	0	NO MEANING
PLATINUM	0	1	0	NO MEANING
BURST+	1	1	1	1=1024, 0=256
PLATINUM+	0	1	1	1=1024, 0=256

A.4 CSR3 - Node Information

Bit	Function	Name
0	Node Number Count* (Valid After a Transmission from the Node)	NN0
1		NN1
2		NN2
3		NN3
4		NN4
5		NN5
6		NN6
7		NN7
8	Node ID Number*	NID0
9		NID1
10		NID2
11		NID3
12		NID4
13		NID5
14		NID6
15		NID7

* When ID_MUX CSR8[0] is set:
CSR8[7:0] = Transmit AGE
CSR8[15:8] = Receive ID.

A.5 CSR4 - Interrupt Address (LSP)

Bit	Function	Name
0	Interrupt FIFO Address Field (LSP)	Always = 0
1		Always = 0
2		RFA2
3		RFA3
4		RFA4
5		RFA5
6		RFA6
7		RFA7
8		RFA8
9		RFA9
10		RFA10
11		RFA11
12		RFA12
13		RFA13
14		RFA14
15		RFA15

A.6 CSR5 - Interrupt Address (MSP) and Status (READ Only*)

Bit	Function	Name
0	Interrupt FIFO Address Field (MSP)	RFA16
1		RFA17
2		RFA18
3		RFA19
4		RFA20
5		RFA21
6		RFA22
13-7	Reserved	0
14	Retry Bit in Interrupt FIFO	(RF_RETRY)
15	Interrupt FIFO Not Empty	(~RX_F_E)

* Writing the Transmit Time-out value to CSR5 stores it in shadow memory. Do not set this value to ‘0’. A value of ‘0’ will keep host-provided data from leaving the Transmit FIFO

A.7 CSR6 - ISA Transfer Register

(See Appendix B for more details)

Bit	Function	Name
1-0	**Transaction Type (R/W)**: 00 = Byte Transaction 01 = Shortword Transaction 1X = Longword Transaction	
3-2	Reserved	
5-4	**Page Configuration (R)**:*: 00 = 8 KB 01 = 16 KB 10 = 32 KB 11 = 64 KB	
6	**Page Enable** 1 = ON	
7	**SIMM Enable (R)**: If the configuration software finds SIMMs installed, this bit is set to ‘1’. If no SIMMs are installed, a ‘0’ selects the 128 KB on-board memory option. and a ‘1’ selects the 4 KB option.	
15-8	Reserved	

* These bits are only written from the EEPROM during initialization

A.8 CSR7 - Reserved

Not Used

A.9 CSR8 - General SCRAMNet+ Extended Control Register

Bit	Function	Name
0	1 is CSR3=T_AGE & RXID fields	ID_MUX
1	Disable HOLDOFF feature	DIS_HOLD
2	Chip select to EEPROM	CSR_CS0
3	Ext. Chip Select for AUX MICROWIRE peripheral	CSR_CS1
4	MICROWIRE DOUT pin	CSR_DOUT
5	EEPROM program enable	E_PRE
6	CLK line to MICROWIRE port	CSR_CK
7	DIN line connected to the MICROWIRE DOUT pins	E_DIN
8	Initiate initiation sequence - CSR Reset	CSR_RST
9	Override Counter mode	GPC_FRE
10	Receive Interrupt Override	RX_INT_OVR
11	1 = Mechanical Switch Override 0 = Invoke Mech. Switch Loopback Mode	C_MECHSW
12	Memory Size Configuration (See below)	MCI0
13	Memory Size Configuration (See below)	MCI1
14	Memory Size Configuration (See below)	MCI2
15	Reserved (always 1)	1

Memory Size Configuration

Bit 14	Bit 13	Bit 12	Memory Size
1	1	1	4 KB
1	1	0	128 KB
1	0	1	512 KB
1	0	0	1 MB
0	1	1	2 MB
0	1	0	4 MB
0	0	1	8 MB

A.10 CSR9 - SCRAMNet+ Interrupt-On-Error Mask

Bit	Function	Name
0	Transmit FIFO Full mask	M_TX_F_F
1	Transmit FIFO Not Empty mask	M_TX_F_E
2	Transmit FIFO 7/8 Full Mask	M_TX_F_AF
3	Internal 82 bit BIST shift register output	BIST_STREAM
4	Receiver FIFO Full Mask	M_RX_F_F
5	Protocol Violation mask	M_PV
6	Carrier Detect Fail mask	M_CD_FAIL
7	Bad Message mask	M_BM
8	Receiver Overflow mask	M_RX_OVR
9	Transmitter Retry mask	M_RETRY
10	Transmitter Retry - Time-out	M_RETRY_T_O
11	Redundant Transmit/Receive Fault mask	M_FAULT
12	Interrupt on General Purpose Counter Overflow	M_COUNT_OVR
13	General Purpose Counter/Timer Modes (Below)	M_INC_TRIGS
14	General Purpose Counter/Timer Modes (Below)	M_INC_ERRS
15	Fiber Optic Bypass Not Connected mask	M_FO_BYPASS

General Purpose Counter/Timer Modes

CSR8[9]	CSR9[14]	CSR9[13]	Counter Modes
0	0	0	Count Errors
0	0	1	Count Triggers (1 & 2)
0	1	0	Transit Time
0	1	1	Network Events
1	1	X	Free Run @ 26.66 ns
1	0	1	1.706 µs\w Trig 2 CLR

A.11 CSR10 - Reserved

Not Used

A.12 CSR11 - Reserved

Not Used

A.13 CSR12 - SCRAMNet+ Virtual Paging Register

(Refer to Section 4, paragraph 4.2.1, and Section 5, page 5-15 for additional information)

Bit	Function	Name
0	Enables Virtual Paging when set	VP
4-1	Always ‘0’	0
5	Virtual Page Number	VP_A12
6		VP_A13
7		VP_A14
8		VP_A15
9		VP_A16
10		VP_A17
11		VP_A18
12		VP_A19
13		VP_A20
14		VP_A21
15		VP_A22

A.14 CSR13 - SCRAMNet+ General Purpose Counter Timer

(Refer to Section 4, paragraph 4.9, and Section 5, page 5-16 for additional information)

Bit	Function	Name
0	Counter/Timer register	RD_COUNT[0]
1	Counter/Timer register	RD_COUNT[1]
2	Counter/Timer register	RD_COUNT[2]
3	Counter/Timer register	RD_COUNT[3]
4	Counter/Timer register	RD_COUNT[4]
5	Counter/Timer register	RD_COUNT[5]
6	Counter/Timer register	RD_COUNT[6]
7	Counter/Timer register	RD_COUNT[7]
8	Counter/Timer register	RD_COUNT[8]
9	Counter/Timer register	RD_COUNT[9]
10	Counter/Timer register	RD_COUNT[10]
11	Counter/Timer register	RD_COUNT[11]
12	Counter/Timer register	RD_COUNT[12]
13	Counter/Timer register	RD_COUNT[13]
14	Counter/Timer register	RD_COUNT[14]
15	Counter/Timer register	RD_COUNT[15]

A.15 CSR14 - ISA Page Select Register

(See Appendix B for more details)

Bit	Function	Name
0	LSB	
1		
2		
3		
4	Page Select Register*	
5		
6		
7		
8		
9	MSB	
15-10	Reserved	

* These bits are only used when CSR6 is set.

A.16 CSR15 - Reserved

Not Used

A.17 Auxiliary Control RAM (R/W)

Bit	Function	Name
0	Receive Interrupt Enable	RIE
1	Transmit Interrupt Enable	TIE
2	External Trigger 1 (Host Read/Write)	ET1
3	External Trigger 2 (Network Write)	ET2
4	HIPRO	HIPRO
7-5	Reserved	0

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APPENDIX B
ISA CSR SUMMARY

B.1 CSR6 - ISA Transfer Register

This register is used to define host data transfer size. It is driven by the **SCRAMNet+** EEPROM.

Bit	R/W	Function
1-0	R/W	Transaction Type: 00 = Byte Transaction 01 = Shortword Transaction 1X = Longword Transaction
3-2	R/W	Reserved
5-4	R*	Page Configuration: 00 = 8 KB 01 = 16 KB 10 = 32 KB 11 = 64 KB
6	R	Page Enable 1 = ON
7	R	SIMM Enable. If the configuration software finds SIMMs installed, this bit is set to ‘1’. If no SIMMs are installed, a ‘0’ selects the 128 KB on-board memory option. and a ‘1’ selects the 4 KB option.
15-8	R	Always read as zero

* These bits are only written from the EEPROM during initialization

EEPROM Initialization:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0					0	0	1	1

Set by configuration software

B.2 CSR14 - ISA Page Select Register

This register is used to set Page Select. This determines window size in memory.

Bit	R/W	Function
0	LSB	Page Select Register*
1		
2		
3		
4		
5	R/W	
6		
7		
8		
9	MSB	
10	R	Reserved. Always read as zero
11		
12		
13		
14		
15		

* These bits are only used when CSR6 is set.

EXAMPLE:

128 KB memory with 8 KB page size.
128 K = 20000 *hex*
8 K = 2000 *hex*

CSR14 = starting address - ending address (**SCRAMNet** Addresses)

Page	Starting Address	Ending address	Page	Starting Address	Ending address
0	0000 -	1FFF	8	10000 -	11FFF
1	2000 -	3FFF	9	12000 -	13FFF
2	4000 -	5FFF	A	14000 -	15FFF
3	6000 -	7FFF	B	16000 -	17FFF
4	8000 -	9FFF	C	18000 -	19FFF
5	A000 -	BFFF	D	1A000 -	1BFFF
6	C000 -	DFFF	E	1C000 -	1DFFF
7	E000 -	FFFF	F	1E000 -	1FFFF

APPENDIX C
SPECIFCATIONS

TABLE OF CONTENTS

C.1 Hardware Specifications

Hardware Compatibility:	ISA 16-bit compliant; IEEE Standard P996 Operates at ISA maximum bus clock speed
Physical Dimensions:	13.4" x 4.8" Card (w/face plate) one slot
Weight:	
ISA Card	0.6 lbs
Media Card, Fiber Optic	0.0915 lbs
Electrical Requirements:	+5 VDC, 1.5 Amps max.
Temperature Range:	
Storage	-40° to +70°C
Operation	0° to +40°C
Humidity Range:	
Storage	0% to 95% (noncondensing)
Operation	10% to 90% (noncondensing)
Network Line Transmission Rate:	150 million bits/second
Message Length:	
Fixed Length:	82 Bits
Variable Length:	46 bits + 256 or 1024 Data Bytes Maximum
Maximum Nodes on Network Ring:	256
Error Correction:	Available in PLATINUM mode only
Maximum Node Separation:	
Coax:	30 meters
Standard Fiber:	300 meters
Long Link Fiber:	3500 meters
Shared Memory:	
ASIC Memory	4 KB
On-board Memory	128 KB
Optional Sizes:	
Low Density SIMMs (512 KB)	512 KB, 1 MB, 2MB
High Density SIMMs (2 MB)	2 MB, 4 MB and 8 MB
Effective Per-Node Bandwidth:	
4 bytes/packet:	6.5 MB/sec
256 bytes/packet:	16.2 MB/sec
1024 bytes/packet:	16.7 MB/sec
Node Latency:	
4 bytes/packet:	250 ns - 800 ns
256 bytes/packet:	250 ns - 16 µs
1024 bytes/packet:	250 ns - 61.8 µs
Internal clock speeds:	
SCRAMNet board crystal	150 MHz, ±100 ppm. [1]
26.66 ns timer is a divide-by-four:	37.5 MHz[2]
1.706 µs timer is a divide-by-256:	585.9 KHz[3]

1. Specifications on the crystal demonstrate the precision and stability of the main clock from which all other clocks are derived. This does not include the vagaries introduced by the circuit.
1. The 37.5 MHz clock is the distributed (on board) clock used by other circuits on most of our host cards.
1. The 585.9 KHz clock is that which is counted by the internal (to ASIC) users timer.

C.2 Bus Voltage Specifications

VOLTAGE NOMINAL	VOLTAGE		CURRENT		VOLTAGE SENSE MIN	PEAK/PEAK NOISE MAX (5)
	MIN	MAX	8 MAX	8/16 MAX		
12	11.4	12.6	1.5 (1)	1.5 (1)	10.8	120 Mv
-12	-10.8 (2)	-13.2 (2)	.3	.3	-10.2	120 Mv
5	4.875 (3)	5.25	3.0	4.5	4.5	50 Mv
-5	-4.5 (4)	-5.5 (4)	.2	.2	-4.3	50 Mv

NOTES:

(1) IEEE P996 specs 1.0
(2) IEEE P996 specs -11.4 and -12.6
(3) EISA specs 4.5
(4) IEEE P996 specs -4.75 and -5.25
(5) PEAK to PEAK noise voltage is defined by the IEEE P996

This table represents the combination of the EISA and IEEE P996 bus specifications. For the cases in which the IEEE P996 bus specification disagrees with the EISA bus specification, the entry placed in the table for voltage is the one closest to the original IBM, PC, XT and AT Technical Reference Manuals.

C.3 Part Number

The ISA board part number is in the form:

H-AS-DISA128-00

where:

CODE	DEFINITION
H	Hardware
AS	Top Level Assembly
D	Standard SCRAMNet+
ISA	ISA Bus
XXX	**Memory (bytes)**
	04K = 4 K
	128 = 128 K
	512 = 512 K
	L2M = 2 M (LOW DENSITY)
	H2M = 2 M (HIGH DENSITY)
	04M = 4 M
	08M = 8 M
X	**Transmission Media**
	0 = NO Media Card
	1 = COAX Media Card
	2 = STANDARD FO Media Card
	3 = LONGLINK FO Media Card
	4 = LASERLINK FO Media Card
X	**Variable**. Used for product variations and/or modifications

C.4 Board Dimensions

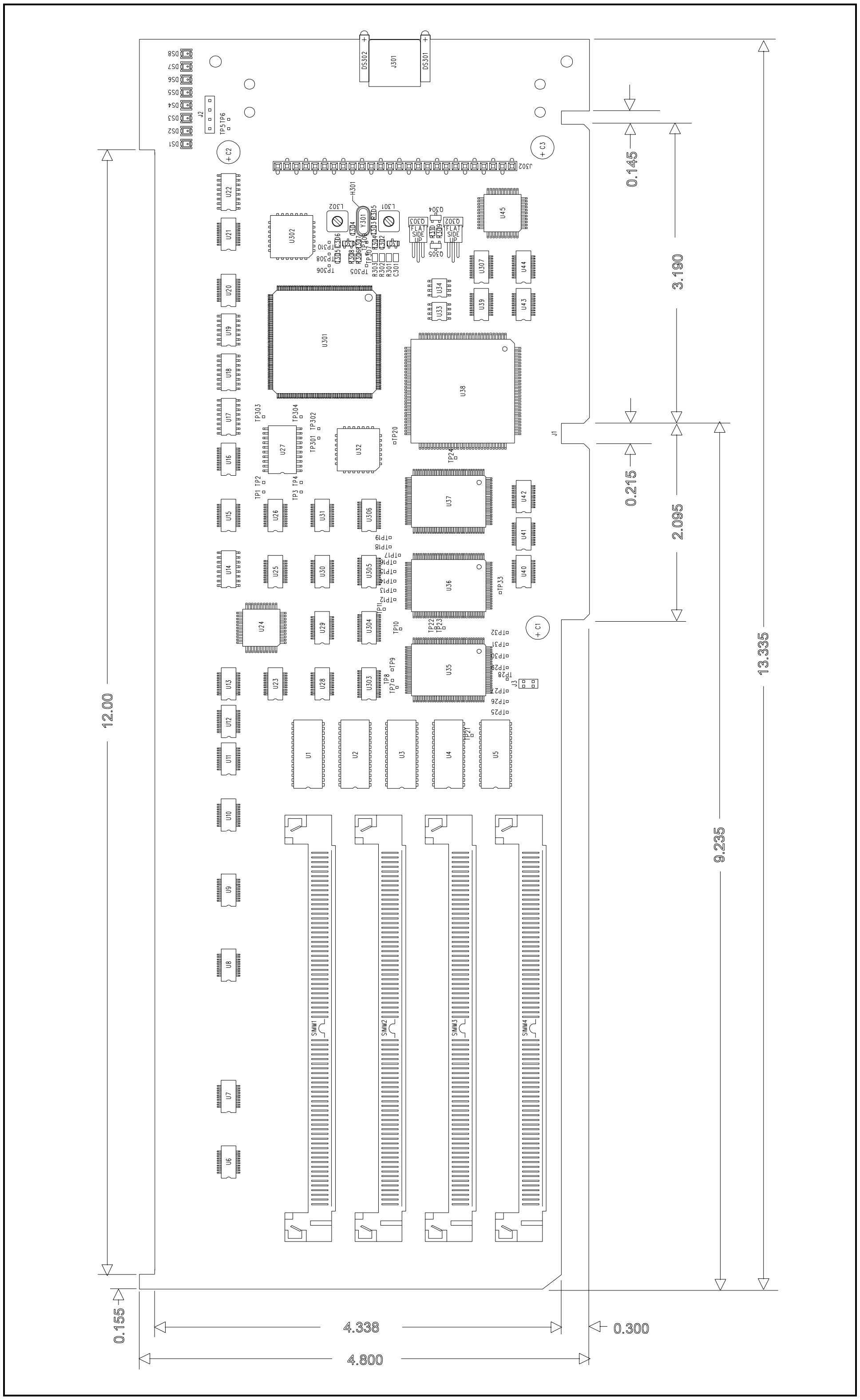
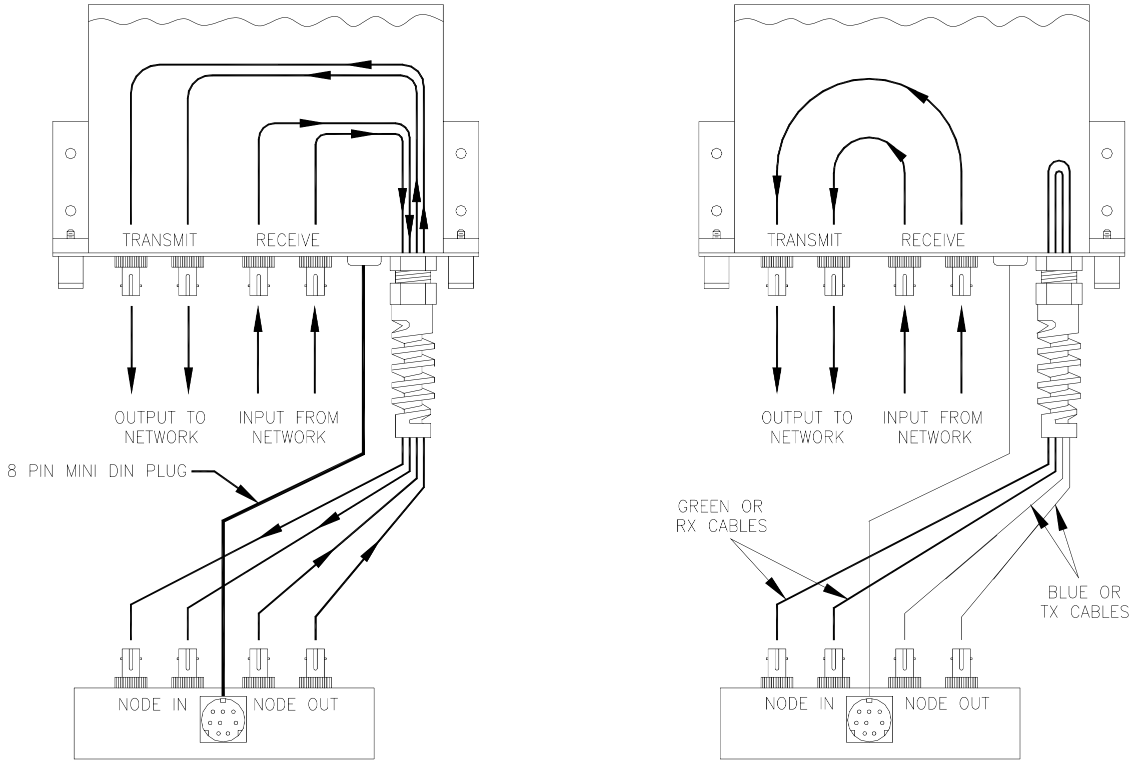


Figure C-1 ISA Board Dimensions

C.5 Fiber Optic Bypass Switch



INSERTED STATE (POWER ON)

BYPASS STATE (POWER OFF)

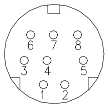
SPECIFICATIONS

OPTICAL PERFORMANCE

INSERTION LOSS	1.2dB TYPICAL, 1.7dB MAXIMUM WITH FOTP 34. 2.5dB MAXIMUM WITH NORMAL MEASUREMENT CRITERIA (AS USED BY CUSTOMER).
LOOPBACK LOSS	3.0dB TYPICAL, 4.0dB MAXIMUM WITH FOTP 34. 6.0dB MAXIMUM WITH NORMAL MEASUREMENT CRITERIA (AS USED BY CUSTOMER).
SWITCHING TIME (POWER LOSS TO POINT THAT RELIABLE DATA TRANSFERS OCCUR)	30MSEC MAXIMUM OVER 4.2 VDC TO 5.0 VDC RANGE.
CROSS-TALK	-60dB MAXIMUM.
DURABILITY	10^7 CYCLES MINIMUM.
REPEATABILITY	0.02dB MAXIMUM.
ALLOWABLE LENGTH DIFFERENCE BETWEEN PRIMARY AND SECONDARY DATA PATHS IN "INSERT" OR "BYPASS" STATE	LESS THAN 6" (.76NS) MEASURED BY SYSTRAN SKEWMETER IN "BYPASS" MODE AT PTX AND STX TO PRX AND SRX. ALSO TX INNER AND OUTER CON' TO RX INNER AND OUTER CON'.
ALLOWABLE SPLICES IN DATA PATH	NONE ON "NEW" UNITS (REPAIRS ON CASE BY CASE BASIS AS CUSTOMER REQUIRES)
OPERATING TEMPERATURE	0°C TO +50°C
STORAGE TEMPERATURE	-20°C TO +60°C
HUMIDITY	40°C/90% RH/5 DAYS

RECEPTACLE PIN ASSIGNMENTS

1	PRIMARY/SECONDARY SWITCH GROUND
2	NO CONNECT/RESERVED
3	PRIMARY/SECONDARY SWITCH POSITIVE
4	NO CONNECT/RESERVED
5	NO CONNECT/RESERVED
6	NO CONNECT/RESERVED
7	NO CONNECT/RESERVED
8	NO CONNECT/RESERVED



NOTES:
1. INSERTION LOSS MEASUREMENTS ARE BASED ON FOTP 34, METHOD B- STEADY STATE EQUILIBRIUM LIGHT LAUNCH CONDITIONS.
2. UNIT CONFIGURED USING ST CONNECTOR RECEPTACLES AND ST CONNECTOR PLUGS.
3. LED WILL BE "ON" WHEN IN INSERTED STATE (POWER "ON").

ELECTRICAL PERFORMANCE

SWITCHING VOLTAGE	3.8 VDC MINIMUM VOLTAGE TO SWITCH THE RELAY
SWITCHING CURRENT (SYSTRAN USES 2 RELAYS IN PARALLEL)	195MA TO 205MA (18.5 TO 19.5 OHMS COIL RESISTANCE + 2 OHMS CABLE AND CONTACT RESISTANCE @ 4.2V)
CONNECTOR	8 PIN MINI DIN PLUG

SYSTRAN CORP.
4126 LINDEN AVE. SUITE 100
DAYTON, OHIO 45432

SIZE	DWG. NO.	REV.
A	A-D-PR-FORELAY-50	D

FILE: FORELAY2.DWG

SHEET 2 OF 4

Figure C-2 Fiber Optic Bypass Switch

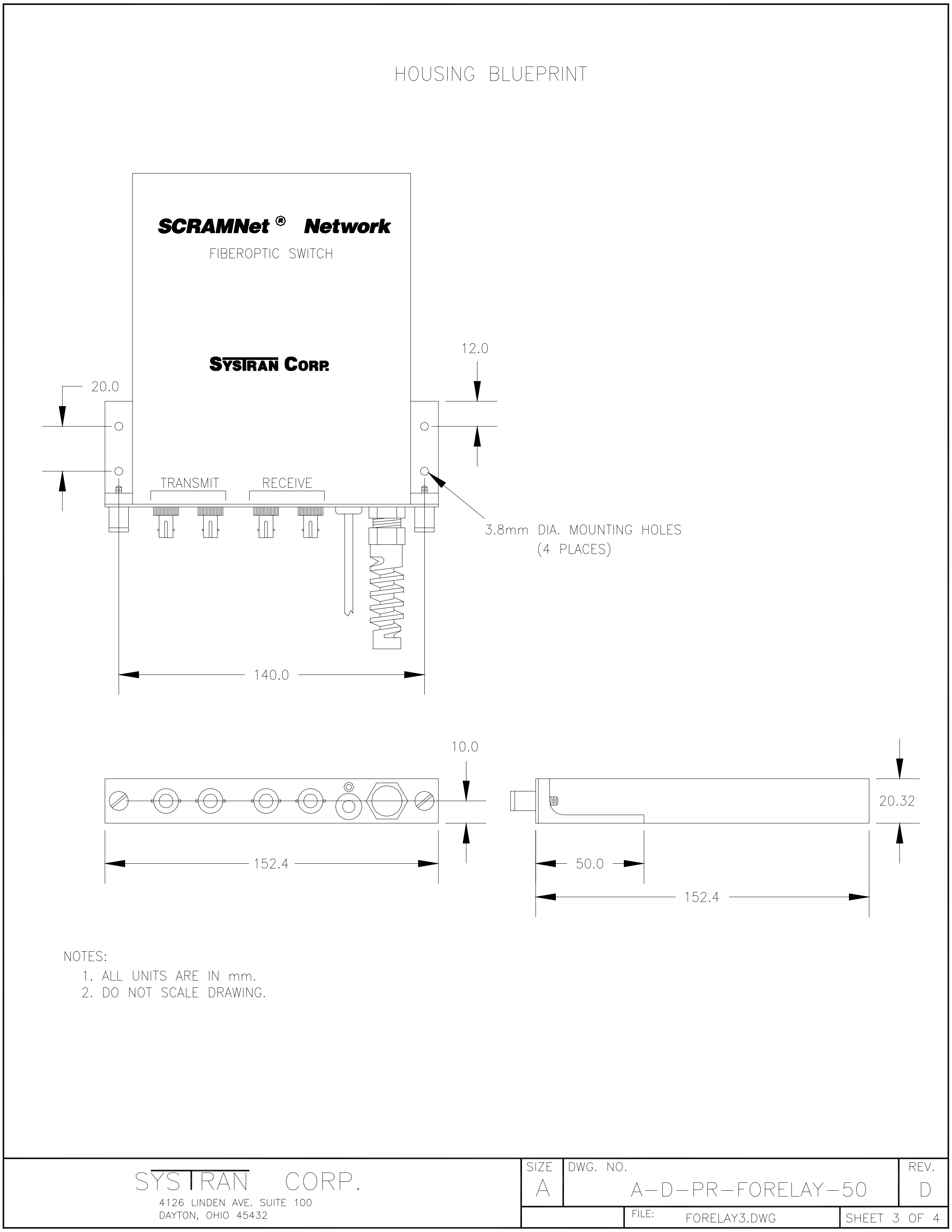


Figure C-3 Housing Dimensions

APPENDIX D
CONFIGURATION AIDS

SCRAMNet+ CONTROL/STATUS REGISTERS REFERENCE SHEET

CSR 0

0	RX ENB
1	TX ENB
2	REDUND LINK TOGGLE
3	HOST INT ENB
4	AUX CTRL RAM ENB
5	INT MEM MASK MATCH
6	OVRD RIE FLAG
7	INT ON ERRORS
8	NET INT ENB
9	OVRD TIE FLAG
10	ENB TX DATA FILTER
11	ENB LOWER 4K FILTER
12	RST TX/RX FIFO
13	RST INT FIFO
14	RST TX FIFO
15	INSERT NODE

CSR 2

0	available to host
1	available to host
2	available to host
3	available to host
4	available to host
5	available to host
6	DSB FO LPBCK
7	ENB WIRE LPBCK
8	DSB HOST TO SM WRT
9	ENB WRT OWN SLOT
10	ENB INT RX OWN SLOT
11	MSG LENGTH LIMIT
12	VAR LENGTH MSGS
13	ENB HIPRO WRITE
14	MULT NATIVE MSGS
15	NO NTWK ERR CRCT

CSR 4

0	always 0
1	always 0
2	RFA 2
3	
4	
5	RX FIFO ADDRESS FIELD
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	RFA 15

CSR 6

0	transaction type
1	transaction type
2	reserved
3	reserved
4	Page Configuration
5	Page Configuration
6	Page Enable
7	SIMM
8	reserved
9	reserved
10	reserved
11	reserved
12	reserved
13	reserved
14	reserved
15	reserved

ACR

0	RIE	4	HIPRO ENB
1	TIE	5	reserved
2	EXT TRG 1	6	reserved
3	EXT TRG 2	7	reserved

LED STATUS

G	INSERT
G	CARRIER DETECT

CSR 1 (READ RESET)

0	TX FIFO FULL
1	TX FIFO NOT EMPTY
2	TX FIFO 7/8 FULL
3	always 0
4	INT FIFO FULL
5	PROTOCOL VIOLATION
6	CARRIER DETECT FAIL
7	BAD MESSAGE
8	RX OVERFLOW
9	TX RETRY
10	TX RETRY TIME-OUT
11	REDUND TXRX FAULT
12	GP CTR/TIMER OVRFLO
13	CURRENT LINK FOR USE
14	INTERRUPTS ARMED*
15	FO BYPASS NOT CNCTD

CSR 3

0	NN0
1	
2	NUMBER
3	OF
4	NODES
5	
6	
7	NN7
8	TXID0
9	
10	
11	NODE ID
12	
13	
14	
15	TXID7

CSR 5

0	RFA16
1	
2	RX FIFO
3	ADDRESS
4	(MSW)
5	
6	RFA22
7	reserved
8	reserved
9	reserved
10	reserved
11	reserved
12	reserved
13	reserved
14	RF RETRY
15	INT FIFO NOT EMT

CSR 7

0	reserved
1	reserved
2	reserved
3	reserved
4	reserved
5	reserved
6	reserved
7	reserved
8	reserved
9	reserved
10	reserved
11	reserved
12	reserved
13	reserved
14	reserved
15	reserved

* Write to CSR1 to re-arm interrupts.

	CSR 8
0	AGE & RXID MUX
1	HOLDOFF DISABLE
2	CHP SELECT EEPROM
3	AUX MICROWIRE
4	MICROWIRE DOUT
5	EEPROM PROG ENABLE
6	MICROWIRE CLOCK LN
7	MICROWIRE DOUT DIN
8	INIT ASIC/CSR RESET
9	GP CTR FREE
10	RX INT OVERRIDE
11	MECH SW OVR
12	MEM SIZE
13	MEM SIZE
14	MEM SIZE
15	Reserved

	CSR 10
0	Not Used
1	Not Used
2	Not Used
3	Not Used
4	Not Used
5	Not Used
6	Not Used
7	Not Used
8	Not Used
9	Not Used
10	Not Used
11	Not Used
12	Not Used
13	Not Used
14	Not Used
15	Not Used

	CSR 12
0	VIRT PG ENB
1	always 0
2	always 0
3	always 0
4	always 0
5	VPA 12
6	
7	
8	VIRTUAL
9	PAGE
10	NUMBER
11	
12	
13	
14	
15	VPA 22

	CSR 14
0	Page Select
1	Page Select
2	Page Select
3	Page Select
4	Page Select
5	Page Select
6	Page Select
7	Page Select
8	Page Select
9	Page Select
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

	CSR 9
0	TX FIFO FULL MASK
1	TX FIFO NOT EMP MASK
2	TX FIFO 7/8 FULL MASK
3	BIST STREAM (R/O)
4	RX FIFO FULL MASK
5	PROTOCOL VIOL MASK
6	CARRIER DETECT FAIL MASK
7	BAD MESSAGE MASK
8	RX OVERFLOW MASK
9	TX RETRY MASK
10	TX RETRY TIME-OUT
11	REDUN TXRX FAULT MASK
12	GP CTR/TIMER OVRFLO
13	UTIL CTR MODES
14	UTIL CTR MODES
15	FO BYPASS NOT CNCTD MASK

	CSR 11
0	Not Used
1	Not Used
2	Not Used
3	Not Used
4	Not Used
5	Not Used
6	Not Used
7	Not Used
8	Not Used
9	Not Used
10	Not Used
11	Not Used
12	Not Used
13	Not Used
14	Not Used
15	Not Used

	CSR 13
0	RD COUNT 0
1	
2	
3	
4	GENERAL
5	PURPOSE
6	COUNTER/
7	TIMER
8	REGISTER
9	
10	
11	
12	
13	
14	
15	RD COUNT 15

	CSR 15
0	reserved
1	reserved
2	reserved
3	reserved
4	reserved
5	reserved
6	reserved
7	reserved
8	reserved
9	reserved
10	reserved
11	reserved
12	reserved
13	reserved
14	reserved
15	reserved

SCRAMNet+ NETWORK CONFIGURATION DATA SHEET

NODE ID	HOST MACHINE	MEMORY ADDRESS & BUS	MEMORY SIZE	CSR ADDRESS & BUS	INT LEVEL	SCRAMNet SERIAL #

APPENDIX E
ISA CONFIGURATION MANAGER

Table of Contents

E.1 Overview

The **SCRAMNet** Configuration Program (**scr_cm**) is a **SCRAMNet** utility designed to simplify the process of configuring a **SCRAMNet** card's default resource assignments, and provide some control over the functional capabilities of the card.

This program is based on the EPI program distributed with other hardware implementations of **SCRAMNet**. Therefore this program will appear identical to the EPI program except for the addition of some additional menu choices.

This section will provide detailed instruction about the menu choices unique to the **scr_cm** program and refer you to the utilities manual for those parts common to both this program and the EPI program.

E.2 Calling Syntax

scr_cm	Run the interactive version of the program.
scr_cm -notitle	Disable display of the scrolling logo.
scr_cm -serial hexvalue	Run interactive version of program with the serial number set to the given hexadecimal value.
scr_cm -auto	Non-interactively initialize the device with default values.
scr_cm -auto hexvalue	Initialize with default values and serial number set to hexvalue.
scr_cm -init	Send software reset signal to card. This will reset the contents of the configuration registers to there default state.
scr_cm -read hexvalue	Allows program to force the Plug-and-Play read-data-port location to a value other than the default location of 207 *hex*
scr_cm -status	Display current Plug-and-Play configuration settings.
scr_cm -active	Place **SCRAMNet** card in active mode.
scr_cm -regs v0 v1 v2 v3 v4 v5 v6 v7 v8 v9 v10 v11 v12 v13 v14 v15	This option allows for non-interactive setting of the EEPROM. The value for each of the 16 registers (v0..v15) must be listed (in hex) after -regs
scr_cm -activate_default	Reset device to default values and activate.

E.3 Locating the SCR_CM Program

Change to the directory in which you installed the **SCRAMNet** software. The **scr_cm** program will be in the *cfg* subdirectory.

NOTE: In order to move the executable to another location, you must also copy the **scr_cm.hlp** file and **hostreg.def** file to the new location.

E.4 Interactive Mode

When running the program in interactive mode, the logo screens will be displayed. Then the software programmable switch settings will be read from the card, and if necessary, the switches will be reprogrammed to allow access to the **SCRAMNet** EEPROM and SIMM modules. Next, the **SCRAMNet** EEPROM and the ISA Plug-and-Play Configuration EEPROM will be read, and the values will be used as the default values presented in the interactive environment.

Once all of the necessary system information has been obtained, the main menu will display. The main menu has five choices as follows:

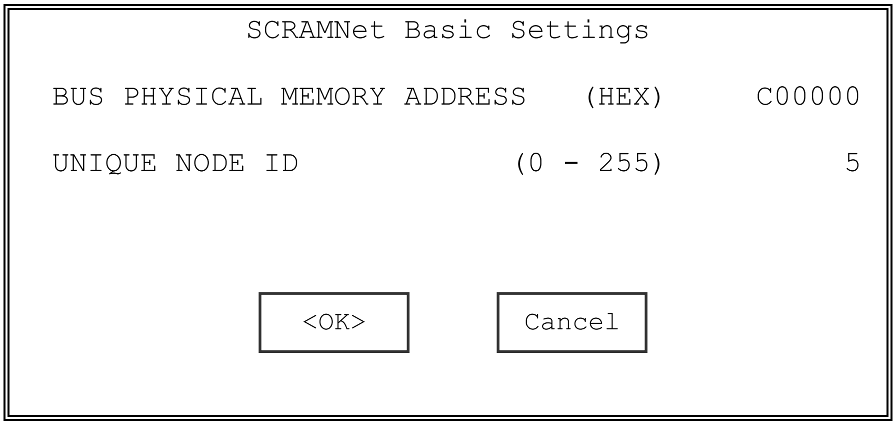
```
                 Main Menu
                Basic Setup
      Edit SCRAMNet CSR Registers (HEX)
    Edit SCRAMNet CSR Registers (Bitwise)
         Edit ISA Configuration Data
                    Quit
```

The first three options are described in detail in the **epi** section of the **SCRAMNet** Utilities User manual. Therefore this section only provides a brief example of what these dialog windows will look like.

NOTE: See the *SCRAMNet Utilities User Manual* for detailed instructions

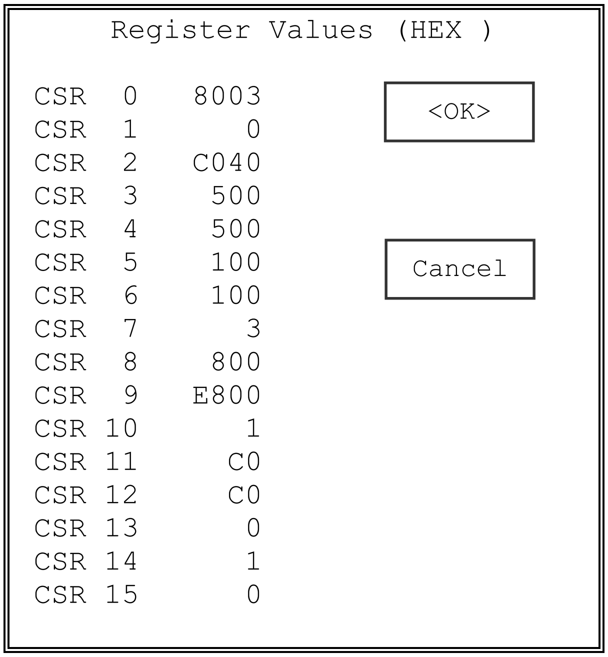
E.5 Basic Setup

Selecting “Basic Setup” will cause the Basic settings window to Display as shown below:



```
                SCRAMNet Basic Settings

BUS PHYSICAL MEMORY ADDRESS    (HEX)      C00000

UNIQUE NODE ID              (0 - 255)          5
```

E.5.1 Edit Registers (HEX)



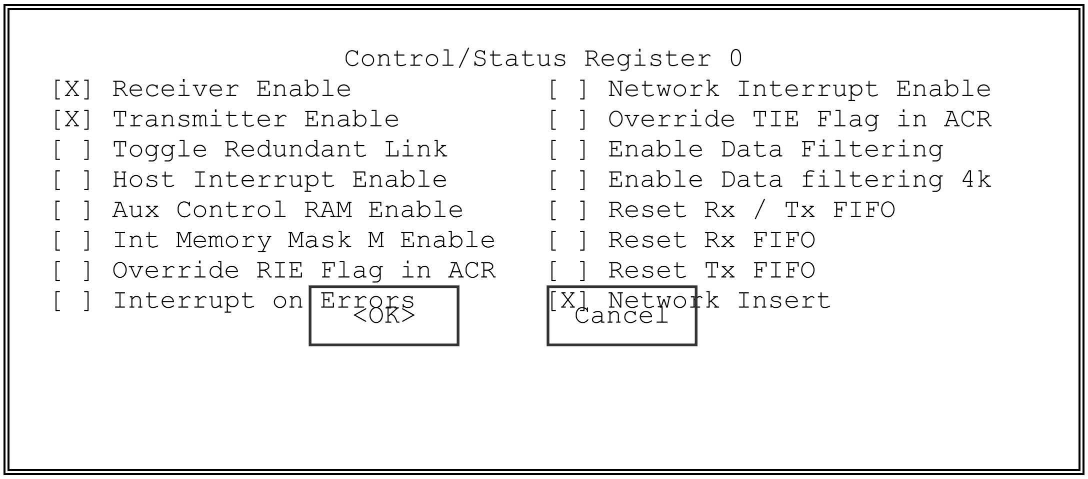
```
   Register Values  (HEX )

CSR  0   8003
CSR  1      0
CSR  2   C040
CSR  3    500
CSR  4    500
CSR  5    100
CSR  6    100
CSR  7      3
CSR  8    800
CSR  9   E800
CSR 10      1
CSR 11     C0
CSR 12     C0
CSR 13      0
CSR 14      1
CSR 15      0
```

NOTE: CSR3 and CSR4 store the default power-up TX and RX ID’s for **SCRAMNet**. Ensure that both values for CSR3 and CSR4 are identical.

WARNING: CSR5 controls the network time-out for **SCRAMNet**. Do not write a zero value for CSR5 or host generated messages will not be able to leave the

Transmit FIFO. See Section 5.0 CSR DESCRIPTIONS for more information.

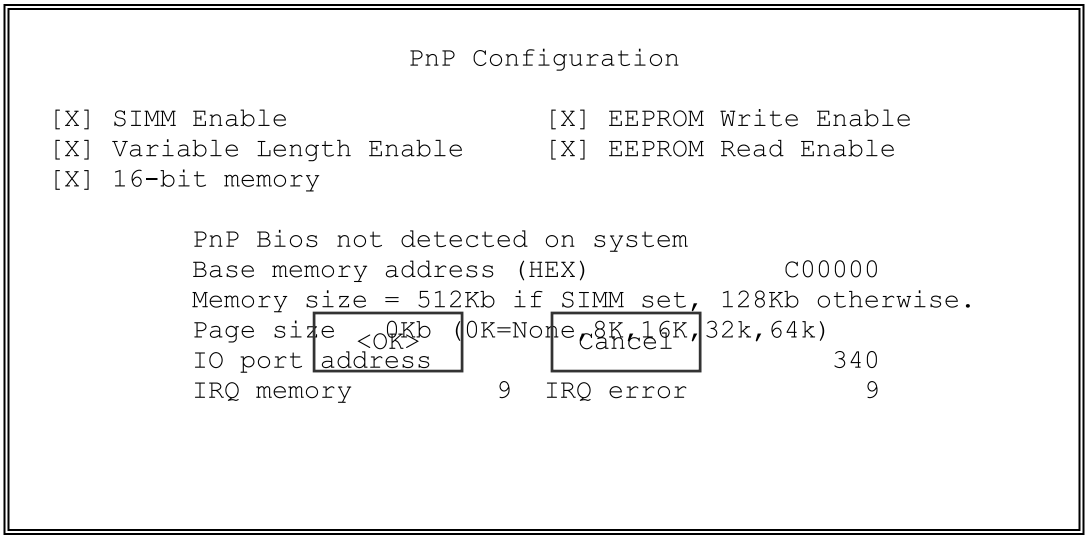
E.5.2 Edit Registers Bitwise



```
                    Control/Status Register 0
[X] Receiver Enable                [ ] Network Interrupt Enable
[X] Transmitter Enable             [ ] Override TIE Flag in ACR
[ ] Toggle Redundant Link          [ ] Enable Data Filtering
[ ] Host Interrupt Enable          [ ] Enable Data filtering 4k
[ ] Aux Control RAM Enable         [ ] Reset Rx / Tx FIFO
[ ] Int Memory Mask M Enable       [ ] Reset Rx FIFO
[ ] Override RIE Flag in ACR       [ ] Reset Tx FIFO
[ ] Interrupt on Errors            [X] Network Insert
```

E.6 ISA Configuration Data

Selecting ISA configuration Data causes the following window to be displayed:



```
                        PnP Configuration

[X] SIMM Enable                    [X] EEPROM Write Enable
[X] Variable Length Enable         [X] EEPROM Read Enable
[X] 16-bit memory

         PnP Bios not detected on system
         Base memory address (HEX)            C00000
         Memory size = 512Kb if SIMM set, 128Kb otherwise.
         Page size   0Kb (0K=None,8K,16K,32k,64k)
         IO port address                         340
         IRQ memory         9  IRQ error           9
```

This window allows new default resources to be specified for the **SCRAMNet** Card. The series of toggle buttons at the top of the window show the current digital switch settings.

The 16-bit memory toggle button is used to determine if memory is 16-bit or 8-bit. The SIMM enable button allows the user to specify if the card should use the 128 KB of on-board memory or whatever memory is in the SIMM slots.

When the **scr_cm** program is executed, the SIMM-enable jumper is toggled ON so that the board can detect the amount of memory available in the SIMM slots. When displayed, the ISA Configuration screen is updated to show the amount of memory available for each position of the SIMM jumper as described in Table E-1.

Table E-1 SIMM Jumper Options

SIMM Jumper	SIMM Memory Present?	Result
ON	Yes	Use memory in SIMM slots
ON	No	Use 4 KB Internal ASIC Memory
OFF	No	Use 128 KB on-board memory

The base-memory address is the physical bus address for the shared memory. The location of this address can be any value in one of two ranges. When paging is enabled, the base address must be below 1 MB, so the base-memory address is limited to values in the range of D0000 *hex* to FFFFF *hex*. When paging is disabled, then the base address can be placed in upper memory anywhere in the range of 100000 *hex* to FFFFFF *hex*. The **SCRAMNet** card is put in paging mode whenever a page size other than zero is selected.

NOTE: The base address must be an even multiple of the page or memory size.

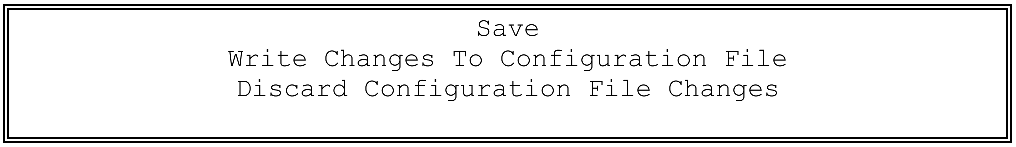
The I/O port address is the location at which the **SCRAMNet** CSR registers will be mapped. This address can be any value in the range 200 *hex* - 380 *hex* in 64 Byte (40 *hex*) increments.

The IRQ settings can be any of the following values 3,4,5,6,7,9,10,11,12,14,15 or 0 for none.

When all the desired changes have been made, press the OK button. The program will verify that the information presented is valid, and attempt to detect possible conflicts with other system devices. If an error is detected, a message window will appear describing the problem, and the cursor will be placed back in the field in question.

E.7 Exiting the Program

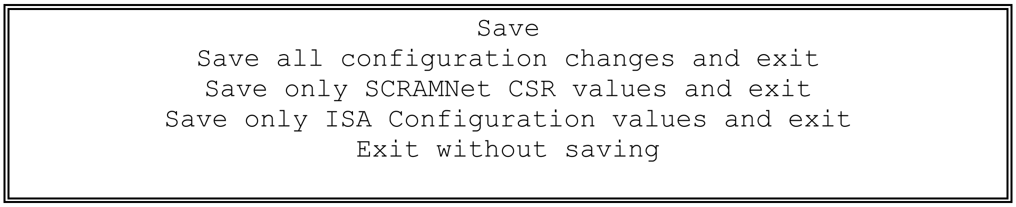
Control returns to the main menu when all initialization information has been entered. The next step is to select <Quit> which presents the option to save the information to the **scrcfg.dat** configuration file. The configuration file and EEPROM may contain different values if the data is not written.



```
                         Save
         Write Changes To Configuration File
         Discard Configuration File Changes
```

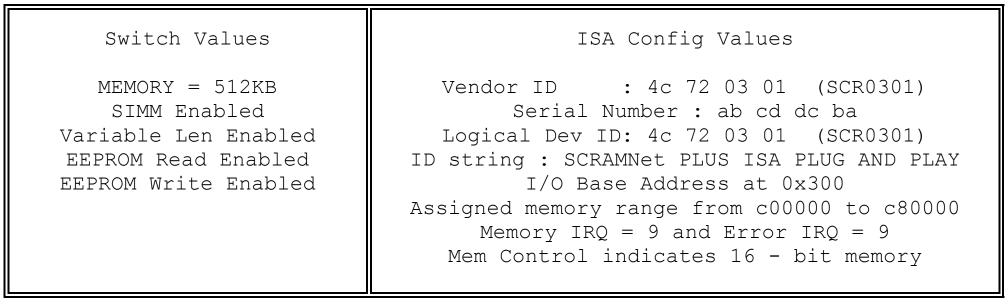
The last option before quitting **scr_cm** is save the **SCRAMNet** EEPROM, ISA configuration data, both, or none. To save only the **SCRAMNet** EEPROM values select ‘Save only SCRAMNet CSR values and exit’. To save only the ISA configuration data select ‘Save only ISA Configuration values and exit’.

NOTE: When making changes to the paging option it is necessary to write both the **SCRAMNet** EEPROM and ISA configuration data. Therefore, when the program detects a change in the page settings it will save all configuration changes unless you exit without saving anything.

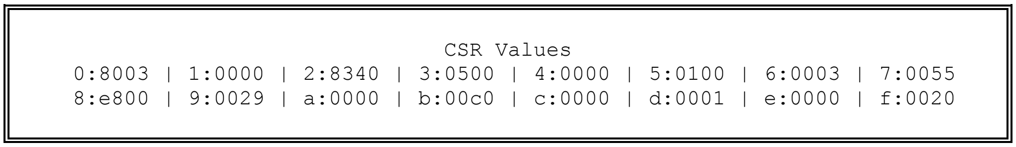


```
                         Save
         Save all configuration changes and exit
          Save only SCRAMNet CSR values and exit
      Save only ISA Configuration values and exit
                  Exit without saving
```

While the program is writing configuration data, it will display the values to be written in a series of windows similar to the following.



```
     Switch Values                            ISA Config Values

   MEMORY = 512KB              Vendor ID     : 4c 72 03 01  (SCR0301)
     SIMM Enabled                   Serial Number : ab cd dc ba
 Variable Len Enabled          Logical Dev ID: 4c 72 03 01  (SCR0301)
  EEPROM Read Enabled       ID string : SCRAMNet PLUS ISA PLUG AND PLAY
 EEPROM Write Enabled                I/O Base Address at 0x300
                            Assigned memory range from c00000 to c80000
                                 Memory IRQ = 9 and Error IRQ = 9
                               Mem Control indicates 16 - bit memory
```



```
                                  CSR Values
 0:8003 | 1:0000 | 2:8340 | 3:0500 | 4:0000 | 5:0100 | 6:0003 | 7:0055
 8:e800 | 9:0029 | a:0000 | b:00c0 | c:0000 | d:0001 | e:0000 | f:0020
```

E.8 Non-interactive modes

Running the program with one of the following sequences of parameters results in the execution of a series of predefined commands with virtually no user interaction.

E.8.1 ‘scr_cm -auto’

Running **scr_cm** with the **auto** flag configures the card with predefined configuration values for all elements except memory size and serial number. If a SIMM is present on the board, the memory size will be set equal to the amount of memory detected in the SIMM slots. Otherwise, a prompt will display requiring selection of memory size: either 4 KB or 128 KB.

The current serial number will be retained.

While the board is being programmed it will open three windows similar to the following showing the resources that will be programmed.

```
                 SCRAMNet Automated configuration
```

```
     Switch Values                       ISA Config Values

    MEMORY = 512KB            Vendor ID      : 4c 72 03 01  (SCR0301)
     SIMM Enabled                    Serial Number : ab cd dc ba
 Variable Len Enabled         Logical Dev ID: 4c 72 03 01  (SCR0301)
  EEPROM Read Enabled       ID string : SCRAMNet PLUS ISA PLUG AND PLAY
 EEPROM Write Enabled                I/O Base Address at 0x300
                            Assigned memory range from c00000 to c80000
                                  Memory IRQ = 9 and Error IRQ = 9
                               Mem Control indicates 16 - bit memory
```

```
                              CSR Values
 0:8003 | 1:0000 | 2:8340 | 3:0500 | 4:0000 | 5:0100 | 6:0003 | 7:0055
 8:e800 | 9:0029 | a:0000 | b:00c0 | c:0000 | d:0001 | e:0000 | f:0020
```

E.8.2 ‘scr_cm -auto hexvalue’

Placing a hexadecimal value after the auto switch will set the device serial number equal to the value passed on the command line. Otherwise, this combination functions the same as if the number were not there.

E.8.3 ‘scr_cm -status’

Running **scr_cm** with the **status** flag will cause the active configuration data from the Plug-and-Play controller to be displayed as follows:

```
Current values are :
Vendor ID                  : 4c 72 03 01  (SCR0301)
Serial Number              : 12 34 56 78
Check Sum                  : 11
Logical Device ID          : 4c 72 01 04  (SCR0104)
Device Description         : SCRAMNet PLUS ISA PLUG AND PLAY
IO Base Address = 0x0240
IRQ 0 Level = 09      IRQ 1 Level = 09
Assigned Memory range = 0xc00000 - 0xd00000
Mem Control indicates  16 - bit memory
Device not in Active mode
```

E.8.4 ‘scr_cm -active’

The active flag is a very important flag. By default the program leaves the device in an inactive state. While the device is in the inactive state it is prevented from driving or responding to signals on the ISA bus. The **SCRAMNet** card is intentionally forced into this inactive state so that if it causes a conflict with another device, the other device will continue to function properly until the **SCRAMNet** card is activated.

The **SCRAMNet** card is activated by running the **scr_cm** program with the single flag ‘-active.’

E.8.5 ‘scr_cm -activate_default’

Plug-and-Play systems can alter a device’s active configuration so that it does not match the systems default values. The activate_default flag will reset the **SCRAMNet** card to its default power-up values, and then activate the device.

NOTE: The board is left in the inactive state when exiting **scr_cm** unless either the ‘-active’ or ‘-activate’ flag is specified.

APPENDIX F
GLOSSARY

A16	A type of module that provides or decodes an address on address lines A01 through A15.
A24	A type of module that provides or decodes an address on address lines A01 through A23.
A32	A type of module that provides or decodes and address on address lines A01 through A31.
ACR	Auxiliary Control RAM. A memory buffer typically used as a data bus width extension for control purposes only. Also referred to as shadow memory .
address-only cycle	A DTB cycle that consists of an address broadcast, but no data transfer. The slave does not acknowledge address-only cycles and the master terminates the cycle without waiting for an acknowledgment.
Alarm	Manually resetable latched error condition.
Arbiter	A functional module that accepts bus requests from requester modules and grants control of the DTB to one requester at a time.
Arbitration	The process of assigning control of the DTB to a requester.
arbitration bus	One of the four buses provided by the backplane. This bus allows an arbiter module and several requester modules to coordinate use of the DTB.
arbitration cycle	An arbitration cycle begins when the arbiter senses a bus request. The arbiter grants the bus to a requester, which signals that the DTB is busy. The requester terminates the cycle by taking away the bus busy signal, which causes the arbiter to sample the bus requests again.
Backplane	A printed circuit board (pcb) with 96-pin connectors and signal paths that bus the connector pins. Some systems have a single pcb, called the J1 backplane. It provides the signal paths needed for basic operations. Other systems also have a second pcb, called a J2 backplane. It provides the additional 96-pin connectors and signal paths needed for wider data and address transfers. Still others have a single pcb, called a J1/J2 backplane that provides the signal conductors and connectors of both the J1 and J2 backplanes.
backplane interconnect	An internal processor bus that allows I/O device controllers to communicate with main memory and the central processor, or they may be on a separate bus entirely. In the latter case, the I/O board enables and controls the communications between the I/O bus and the processor and memory.
backplane interface logic	Special logic that takes into account the characteristics of the backplane: its signal line impedance, propagation time, termination values, etc. The specification prescribes certain rules for the design of this logic based on the maximum length of the backplane and its maximum number of board slots.
bad message	A message error condition reported by a node's receiver circuitry. This condition is automatically corrected by **SCRAMNet+** hardware.
BIOS	Basic Input/Output System.
block read cycle	A DTB cycle used to transfer a block of 1 to 256 bytes from a slave to a master. This transfer is done using a string of 1-, 2-, or 4-byte data transfers. Once the block transfer is started, the master does not release

	the DTB until all of the bytes have been transferred. It differs from a string of read cycles in that the master broadcasts only one address and address modifier (at the beginning of the cycle.) Then the slave increments this address on each transfer so that the data for the next cycle is retrieved from the next higher location.
block write cycle	A DTB cycle used to transfer a block of 1 to 256 bytes from a master to a slave. The block write cycle is very similar to the block read cycle. It uses a string of 1-, 2-, or 4-byte data transfers and the master does not release the DTB until all of the bytes have been transferred. It differs from a string of write cycles in that the master broadcasts only one address and address modifier (at the beginning of the cycle). Then the slave increments this address on each transfer so that the next transfer is stored in the next higher location.
board	See printed circuit board (pcb).
burst	A protocol where messages are transmitted without error correction to gain higher throughput.
burst+	Also **burst plus**. A variable packet size enhancement for the burst protocol. Maximum packet size may be set to either 256 bytes or 1024 bytes.
bus timer	A functional module that measures the time each data transfer takes on the DTB and terminates the DTB cycle if a transfer takes too long. Without this module, it could wait forever for a slave to respond if the master tries to transfer data to or from a nonexistent slave location. The bus timer prevents this by terminating the cycle.
carrier loss	A hardware failure reported when the incoming light link has failed because it is too weak or nonexistent in one or both fibers from the preceding node.
data filter	A process of comparing host WRITE to shared memory with contents of the specified memory location to eliminate transmission of redundent data and reduce network traffic.
deterministic	Completely predictable message transit time from application to application.
data transfer bus	One of the four buses provided by the backplane. The data transfer bus allows masters to direct the transfer of binary data between themselves and slaves (data transfer bus is often abbreviated DTB).
data-transfer-bus cycle	A sequence of level transitions on the signal lines of the DTB that result in the transfer of an address or an address and data between a master and a slave. There are 34 types of data transfer bus cycles.
DMA	Direct Memory Access transfer. An I/O transfer conducted by a device controller which accesses memory directly and, as a result, can transfer a large volume of data without requesting a processor interrupt after each unit amount. Contrast with programmed I/O (PIO) transfer.
device interrupt	An interrupt received on interrupt priority levels 20-23. Device interrupts can be requested only by devices, controllers, and memories.
DTB	Data Transfer Bus.
edges	Transitions that appear on a signal line.
falling edge	The time during which a signal makes its transition from high to low.

FIFO--------------------------------A data storage method; First In First Out. Also refers to the specific storage area; Transmit FIFO, Interrupt FIFO, etc.

foreign message ------------------A message that is in (passing through) a node other than the one of origin.

functional module----------------A collection of electronic circuitry that resides on one board and works together to accomplish a task.

halfword ---------------------------Any double byte on even 16 bit boundaries.

insert a node ----------------------The act of placing a node on a network for the purpose of transmitting and receiving messages.

interrupt---------------------------An event that changes the normal flow of instruction execution other than an exception or a branch, jump, case or call instruction.

interrupt acknowledge cycle---A DTB cycle, initiated by an interrupt handler, that reads a status/ID from an interrupter. An interrupt handler generates this cycle when it detects an interrupt request from an interrupter and it has control of the DTB.

interrupter ------------------------A functional module that generates an interrupt request on the priority interrupt bus and then provides states/ID information when the interrupt handler requests it.

interrupt handler ----------------A functional module that detects interrupt requests generated by interrupters and responds to those requests by asking for status/ID information.

ISR --------------------------------Interrupt Service Routine**.** A routine executed when a device interrupt occurs.

I/O space--------------------------The regions of host processor physical address space that contain the configuration registers, device control, states registers and data registers. These regions are physically noncontiguous.

latched ----------------------------Data is electrically stored in a circuit until it is needed. A method of coordinating two synchronous events.

location monitor------------------A functional module that monitors data transfers over the DTB to detect accesses to the locations it has been assigned to watch. When an access occurs to one of these assigned locations, the location monitor generates an on-board signal.

locking a page in memory------Making a page ineligible for either paging or swapping. A page stays locked in physical memory until the operating system specifically unlocks it.

longword--------------------------Four bytes (32 bits) of data.

loopback --------------------------A method of transmitting to the same node’s receivers for testing purposes. Applies to both fiber optic and wire media. Also, a test tthat loops tthe outgoing signal back to its source.

master ------------------------------A functional module that initiates DTB cycles to transfer data between itself and a slave module.

message packet -------------------See packet.

native message--------------------A message that is received by the node of origin

node latency-----------------------The time delay at a node before a foreign message can be retransmitted.

pcb ---------------------------------printed circuit board. A collection of electronic components, and either one or two 96-pin connectors that can be plugged into the backplane connectors.

packet ------------------------------A message that travels on the network. The minimum packet consists of 81 bits and 1 start bit. The packet includes five fields: Source ID (8 bits), Age (8 bits), Control (3 bits), Data Address (21 bits), Data (32 bits), and 9 parity bits; one for every 8 bits..

physical address------------------The address used by hardware to identify a location in physical memory or on directly-addressable secondary storage devices (such as disks). A physical memory address consists of a page-frame number and the number of a byte within the page.

platinum ---------------------------A protocol where messages are transmitted as fast as the system will allow with error detection enabled.

platinum+ ------------------------(Also platinum plus). A variable packet size enhancement for the platinum protocol. Maximum packet size may be set to either 256 bytes or 1024 bytes.

power monitor--------------------A functional module that monitors the status of the primary power source to the system and signals when the power has strayed outside the limits required for reliable system operations. Since most systems are powered by an ac source, the power monitor is typically designed to detect drop-out or brown-out conditions on ax lines.

priority interrupt bus-----------One of the four buses provided by the backplane. The priority interrupt bus allows interrupter modules to send interrupt requests to interrupt handler modules, and interrupt handler modules to acknowledge these interrupt requests.

PIO ---------------------------------Programmed I/O transfer. An I/O transfer, primarily conducted by a driver program, that requires processor intervention after each byte or word is transferred. Contrast with Direct Memory Access (DMA) transfer.

protocol violation ----------------A signal error at the physical layer (fiber or coax) resulting from noise on the transmission lines or a result of hardware failure. It can be any one of the following:

- Missing transition for two clock periods on either line
- Parity error
- Framing error

read cycle--------------------------A DTB cycle used to transfer 1-, 2-, 3-, or 4-bytes from a slave to a master. The cycle begins when the master broadcasts an address and an address modifier. Each slave captures this address and address modifier, and checks to see if it is to respond to the cycle. If so, it retrieves the data from its internal storage, places it on the data bus, and acknowledges the transfer. Then the master terminates the cycle.

read-modify-write cycle --------A DTB cycle that is used to both read from, and write to, a slave's byte location(s) without permitting any other master to access that location during that cycle. This cycle is most useful in multi-processing systems where certain memory locations are used to control access to certain systems resources, for example, semaphore locations.

requester	A functional module that resides on the same board as a master or interrupt handler and requests use of the CTB whenever its master or interrupt handler needs it.
retry	A hardware failure condition reported when the first attempt to send a message around the network has resulted in some type of bit error. The message will be retransmitted indefinitely by the originating node until it is received correctly by the originating node. Valid only in error correction mode (PLATINUM.)
retry overflow	A hardware failure condition reported when a second attempt to send a message around the network has failed due to another node corrupting data. This rare condition is most likely caused by dirty fiber optic cable ends, or perhaps the fiber cable is installed with too small a radius.
retry timeout	A hardware failure condition reported when the first attempt to send a message around the network is not received by the originating node within the time out period specified in CSR5. The message will be retransmitted indefinitely by the originating node until it is received correctly by the originating node. Valid only in error correction mode (PLATINUM.)
rising edge	The time during which a signal makes its transition from low to high.
Rx	Abbreviation for receive or receiver.
SCSI	Refers to the American National Standard for Information Systems Small Computer System Interface - 1 (X3.131-1986) or the ANSI Small Computer System Interface - 2 (X3.131-1989). This standard defines mechanical, electrical and functional requirements for attaching small computers to each other and to intelligent peripheral devices.
serial clock driver	A functional module that provides a periodic timing signal that synchronizes the operation of the IEEE 1132* serial bus. Timing specifications for the serial clock driver of the IEEE 1132 are given in Appendix C. Two backplane signal lines are reserved for use by a serial bus. However, the protocols of the serial bus are completely independent of the IEEE 1014, and the inclusion of a serial bus is not a required feature of the IEEE 1014. * IEEE 1132 may not yet be an approved standard.
Shadow memory	Also shadow register. See Auxiliary Control RAM (ACR)
shared memory (SM)	**SCRAMNet** memory physically located on the network board. This dual-ported memory is accessable by the host and the network. A host WRITE to shared memory results in a transmitted WRITE to all **SCRAMNet** nodes at the same relative location.
shortword	16 bits. Also referred to as **halfword**.
signal mnemonics.	Terms used to identify signal line events. (1) An asterisk following the name of signals that are level-significant denotes the signal is true/valid when the signal is low. (2) A asterisk following the name of signals that are edge-significant denotes the actions initiated by that signal occur on the falling edge.
slave	A functional module that detects DTB cycles initiated by a master and, when those cycles specify its participation, transfers data between itself and the master.

slot	A position where a board can be inserted into a backplane. If the system has both a J1 and a J2 backplane (or a combination J1/J2 backplane) each slot provides a pair of 96-pin connectors. If the system has only a J1 backplane, then each slot provides a single 96-pin connector. Also, another name for message packet.
subrack	A rigid framework that provides mechanical support for boards inserted into the backplane, ensuring that the connectors mate properly and that adjacent boards do not contact each other. It also guides the cooling airflow through the system, and ensures that inserted boards do not disengage themselves from the backplane due to vibration or shock.
system clock driver	A functional module that provides a 16 MHz timing signal on the utility bus.
system controller board	A board that resides in slot 1 of the backplane and has a system clock driver, a DTB arbiter, and IACK daisy-chain driver, and a bus timer. Some also have a serial clock driver, a power monitor, or both.
Tx	Abbreviation for transmit or transmitter.
UAT	A master that sends or receives data in an unaligned fashion.
utility bus	One of the four buses provided by the backplane. This bus includes signals that provide periodic timing and coordinate the power-up and power-down of sequence of the system.
write cycle	A DTB cycle used to transfer 1-, 2-, 3-, or 4-bytes from a master to a slave. The cycle begins when the master broadcasts an address and address modifier and places data on the DTB. Each slave captures this address and address modifier, and checks to see if it is to respond to the cycle. If so, it stores the data and then acknowledges the transfer. The master then terminates the cycle.