# VANGUARD VME Bus Analyzer

## TECHNICAL NOTE 9002

## Bus Analyzer Non-Volatile Memory/Data Retention

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### Introduction

**Vanguard VME Analyzer and Exerciser Non-Volatile Memory/Data Retention**
Please be advised as follows regarding the design and operation of the Vanguard VME Advanced Analyzer and Exerciser. Note that all Vanguard Analyzers are the same with respect to hardware. Different features and options are enabled by software license keys.

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### Discussion

There are seven types of memory banks on the Vanguard boards.

Analyzer:

(1) Trace memory 64MB DDR SDRAM
(2) Analyzer FLASH memory 32 MB
(3) Exerciser FLASH memory 16 MB
(4) 64 Mbytes DRAM CPU memory
(5) 1K Non-volatile Serial EEPROM (2 pcs.)
(6) Xilinx Virtex2 3000 FPGA and Xilinx Virtex2 1000 FPGA
(7) 16 MB DDR SDRAM for Target and Exerciser.

(1) The Vanguard is incapable of retaining any information captured from the bus in the trace memory after the 5 Volt power source is interrupted or disconnected either at the VME inputs or the optional front panel inputs. Removing the Vanguard from a slot, results in the total destruction and complete loss of all data temporarily captured and stored in the trace memory of the product.

(2) Analyzer 32MB FLASH memory. The Vanguard Flash memory is used to store FPGA images and firmware. Only the BusView application can update the contents of the flash memory through the front panel connection. The flash memories cannot be updated from the VME bus. No information recorded from the bus is stored in flash and it is not possible for the user to store any recorded information in the FLASH memories. If there is a requirement to erase and restore the flash memory, this can be done by uploading new firmware from the BusView User Interface. As part of any Flash reprogramming procedure, the first part of this is to erase the flash by programming a binary ‘1’ to all bit locations.


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Curtiss-Wright has implemented a flash checksum calculation feature that is available through the User Interface. This calculates a 32 bit check sum for each Flash device. These numbers are calculated each time the command is executed and they are not stored anywhere. Select Tools/Hardware/Checksum in BusView to use this feature.

There is also a feature that clears all types of settings stored in the flash excluding the firmware. This is also available by selecting Tools/Hardware/Checksum in BusView.

(3) Exerciser 16 MB FLASH. Same concerns and procedures as (2), above.

(4) The contents of the CPU RAM is completely lost whenever power is disconnected from the board.

(5) The Vanguard does have a non-volatile EEPROM memory for the purpose of preserving FPGA configuration setup parameters. There is no recorded information from the bus being stored in this EEPROM. The contents of this memory may be destroyed by physically moving SW3-4 to the ON position and powering up the board once. This switch must be set in the OFF position in order to operate the board.

(6) On power up, the FPGAs load the appropriate image from the FLASH memory. The user cannot manually load any information into the Xilinx in any way. The FPGAs do contain some SRAM that is used during operation, but all contents in the FPGAs including the memory are lost when power is disconnected.

(7) The Exerciser CPU and Target memory is used during operation of the exerciser. When power is disconnected from the board, the contents are completely lost.

For additional Tech Support contact Curtiss-Wright Controls Defense Solutions.

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