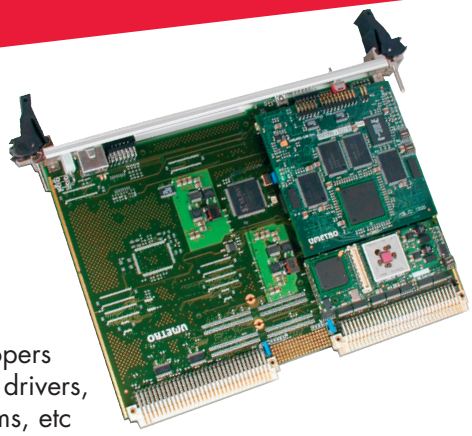
Data Sheet

Vanguard VME

Bus Analyzer, Exerciser & Protocol Checker



The Vanguard VME Bus Analyzer is a complete solution for VMEbus analysis, exercising and protocol error detection in a VME environment. The product includes a 10/100 Mbit/s Ethernet interface, taking the power and flexibility found only in Curtiss-Wright Controls Defense Solutions' range of Bus Analyzers to unprecedented levels of productivity.

Networked VME Bus Analyzer
(built-in Ethernet port)

Allows the user to connect to the Vanguard analyzer at any location where a network connection is available

Supports VME, VME64, 2eVME and 2eSST

Same analyzer for current and future projects

2M Sample Trace Buffer @ 256-bits

Simplifies error location by giving access to large set of sample data

State and Timing Analyzer

Gives a complete trace of all kinds of activity, including arbitration, interrupts, block cycles, RMW etc

Multi-level Trace Viewer

Makes it possible for software and hardware engineers to view the data in their individual preferred views based on the same captured data

Users

- Software developers involved in I/O drivers, operating systems, etc
- System integrators putting together equipment from various vendors
- Hardware designers of interface chips, backplanes and add-in boards

Introduction

The product is the culmination of Curtiss-Wright's two decades of VMEbus design experience. Curtiss-Wright continues to provide engineers with the most effective and powerful tools for debugging, testing and validating next-generation designs.

The unit is controlled via USB or Ethernet from a PC running Windows® and Curtiss-Wright's BusView™ Graphical User Interface (GUI). The Ethernet connection adds a world of possibilities to the Bus Analyzer tool, by allowing the user to connect to the Vanguard analyzers situated at any location where a network connection can be made.

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ABOVE & BEYOND

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Modular Concept

The Vanguard product line consists of many different form factors: VME, PCI, PMC, and CompactPCI (cPCI). The three PCI form factors (PCI, PMC and cPCI) fully support the PCI and PCI-X protocol and signalling, while the VMEbus version supports both legacy VME and the newest 2eVME and 2eSST protocol enhancements. The VME, PCI and cPCI form factors share a common hardware module, called the VG-State Analyzer Module (SAM) module, which is interchangeable between the VME, PCI and cPCI carrier boards. For the PMC form factor a single, fully integrated module has been designed due to the size restrictions imposed by the PMC form factor.

The Vanguard VME is also available in a version (VG-VMEP0) that supports Thales cPCI on P0 pinout. This product has a PMC site available for installation of a Vanguard PMC Bus Analyzer to analyze the PCI bus on the P0 connector.

Figure 1: Vanguard VME Block Diagram

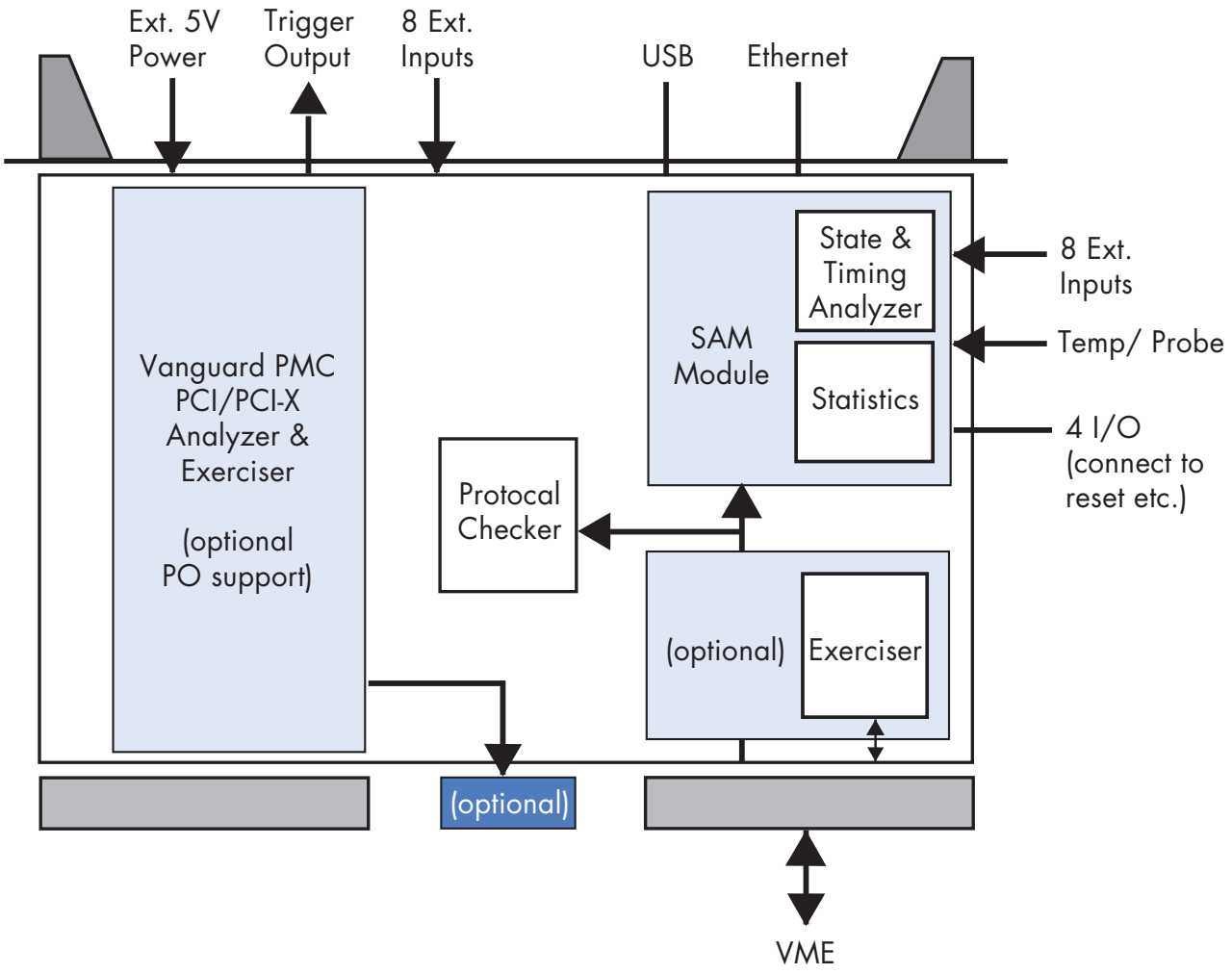


Figure 2: Available Devices and Connection Status

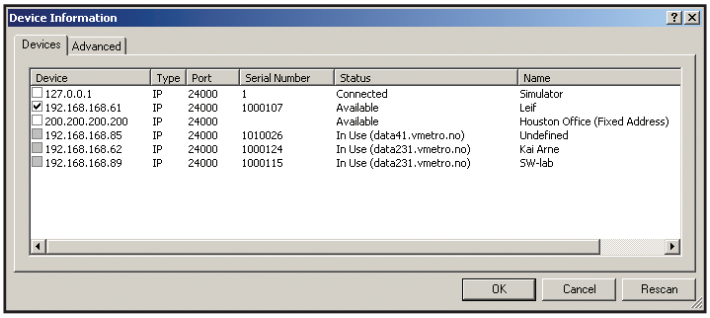


Figure 3: The BusView Graphical User Interface (GUI)

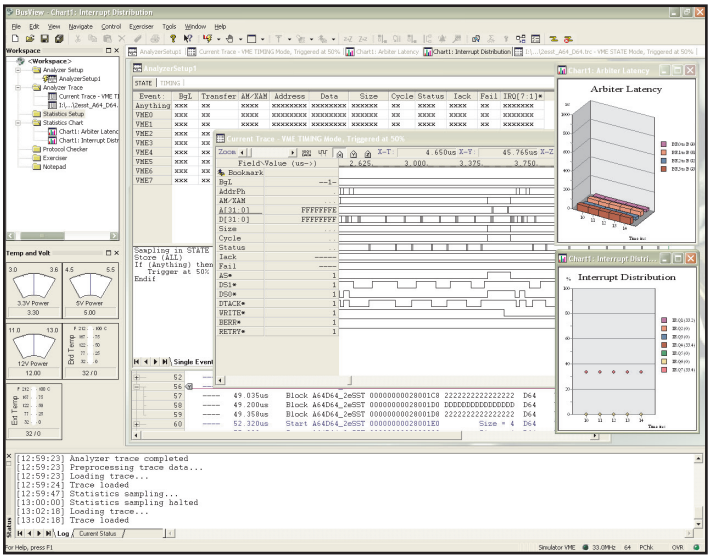
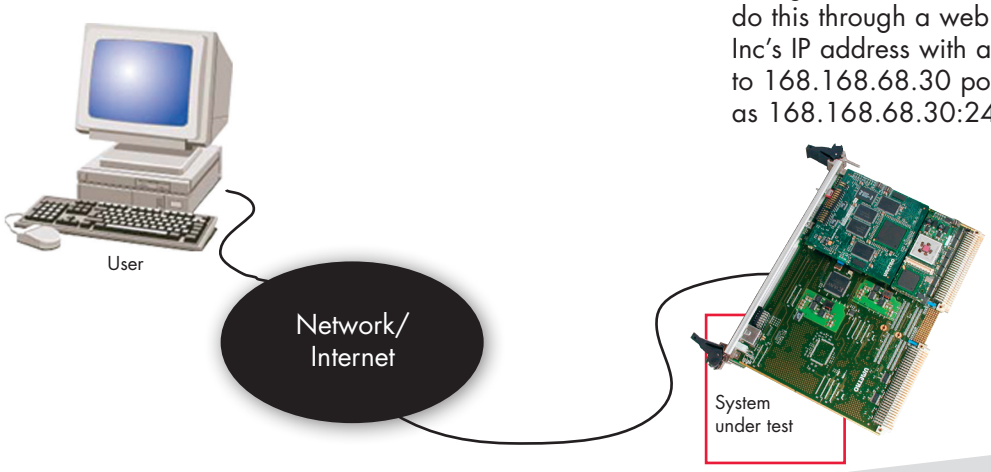


Figure 4: Network Connection



Network Connection

With the introduction of the Vanguard product line, Curtiss-Wright has introduced the Networked Bus Analyzer. By adding an Ethernet port to the Vanguard products the ability to connect a Bus Analyzer to the intranet or internet makes the tool more productive, and introduces new applications for Bus Analyzers as described later.

The Vanguard product will automatically request an IP address from the network's DHCP server if present (if not, an Automatic Private IP Addressing (APIPA) service will be tried as described below). The Vanguard will then be present in the network, and will be available for connection. The user will be able to detect all analyzers present on the local network from a host PC running Windows where the Networked Bus Analyzer GUI is installed as shown in the figure below.

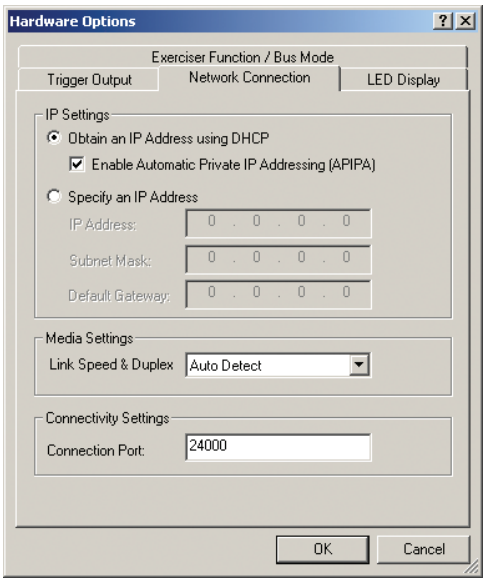
So, in most if not all network architectures (including a point-to-point cross-over Ethernet cable connection between a host PC and a Networked Bus Analyzer), simply connecting an analyzer to the network, inserting it into a system and powering up that system are all that is needed to make it available to all users present on the local network.

It may also be desirable for the user to configure the Vanguard to have a fixed IP address in the network. This is especially useful if the user is accessing the Vanguard via the Internet, and has to go through a Firewall. In order to access the Vanguard inside a Firewall, the Firewall must be configured to route accesses to a specific port number to an IP address inside the network. Let's say ACME, Inc. has an IP address on the internet that is 192.192.192.192. Their local network contains a Networked Bus Analyzer at IP address 168.168.68.30 listening to port 24000. We then configure the Firewall (usually a Network Administrator will do this through a web interface) to route accesses to ACME, Inc's IP address with a specific port number (let's use 1300) to 168.168.68.30 port number 24000 (sometimes written as 168.168.68.30:24000).

APIPA

Automatic Private IP Addressing (APIPA) is a service offered by Windows operating systems that allows a computer to automatically assign itself an IP address in networks where no Dynamic Host Configuration Protocol (DHCP) server is present. APIPA is designed as a failover mechanism for DHCP, and a way to make small local area networks easier to configure. APIPA also allows a Networked Bus Analyzer to be connected directly to a host computer using a cross-over Ethernet cable with no configuration necessary.

Figure 5: Network Connection Settings



The addition of network connectivity to Bus Analyzers opens up several powerful possibilities.

USB

In addition to an Ethernet port, the Vanguard products are equipped with a Universal Serial Bus (USB) port. This widespread, industry standard connection allows fast and convenient connection between the host PC and the Vanguard VME card.

Table 1: Network Connection Settings

Usage	Comment/Benefit
Delocalized connection	The system under test and the user is connected via a network, so the user is free to choose a location that better suits his tasks than being situated in a lab. A software engineer would typically choose to be in his own office.
Sharing of equipment	Since no physical cables need to be swapped, all that is required for one user to give another user access to a Networked Bus Analyzer is for him to close down his GUI connection.
Deployed equipment	A Networked Bus Analyzer can be installed in a deployed system (for example a base station or a radar processing unit), offering an engineer or service technician access to direct measurements on the running system as well as temperature and voltage readings.
Inaccessible systems	Some systems that are being tested or monitored are environments located in specific areas where they are inaccessible (most military vehicles, airplanes and vessels have these areas).
Remote connection	Being able to connect to remote systems allows collaboration work to take place without artificial limitations. A user in Europe can access equipment in a lab in California just as easily as for local equipment.

Advanced Trigger and Store Capabilities

All Vanguard Analyzer products use Curtiss-Wright's unique programming language-like trigger sequencer to specify triggers, store and count and delay qualifiers in an "If-then-else..." fashion. Together with the intuitive demultiplexed sampling method (which puts Address, Data and Status as separate items also in the trigger event specifiers) and true inside/outside range specifiers on address and data fields, the user can easily create sophisticated triggers and store qualifiers without having to use multiple events to define trigger attributes of a single transfer. The user can store trigger setups on the host PC.

A new feature of the Vanguard product family is the graphical sequencer that allows visualization of complex sequences. In sum, all these features allow the user to solve problems quickly, instead of spending hours trying to figure out how to set up and understand the analyzer.

Independent Sub-functions for Concurrent Operation

As can be seen from the block diagrams on page 2, the Vanguard Bus Analyzer products contain a comprehensive set of independent functional units. In essence, this means that there are separate hardware resources for the various functions so that the user, for example, can operate the Exerciser while running the State Analyzer concurrently. This allows for the monitoring of bus traffic results generated by the Vanguard product and other bus agents simultaneously. Furthermore, the Protocol Checker can be run concurrently with the State Analyzer, Exerciser and Real-time Statistics. This offers maximum debugging efficiency, only made possible by the generous use of hardware resources. This approach is in stark contrast with other products where often one or a few common hardware resources are shared for each sub-function, thus restricting which functions may operate at the same time.

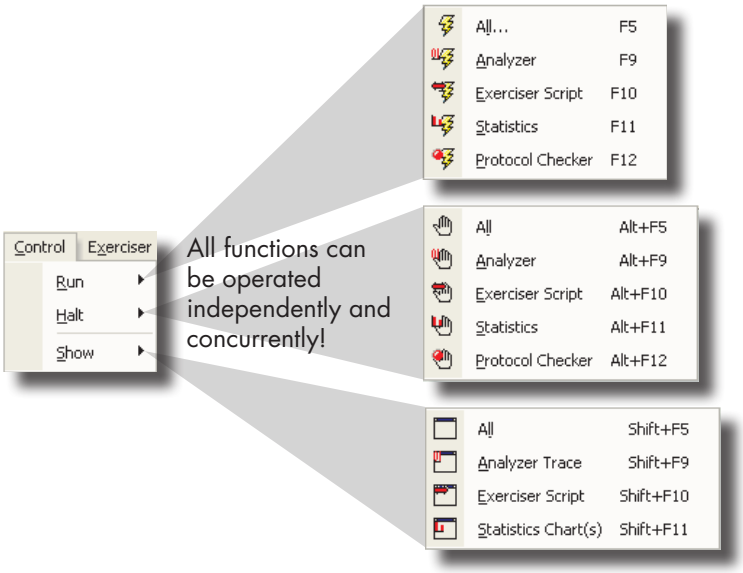
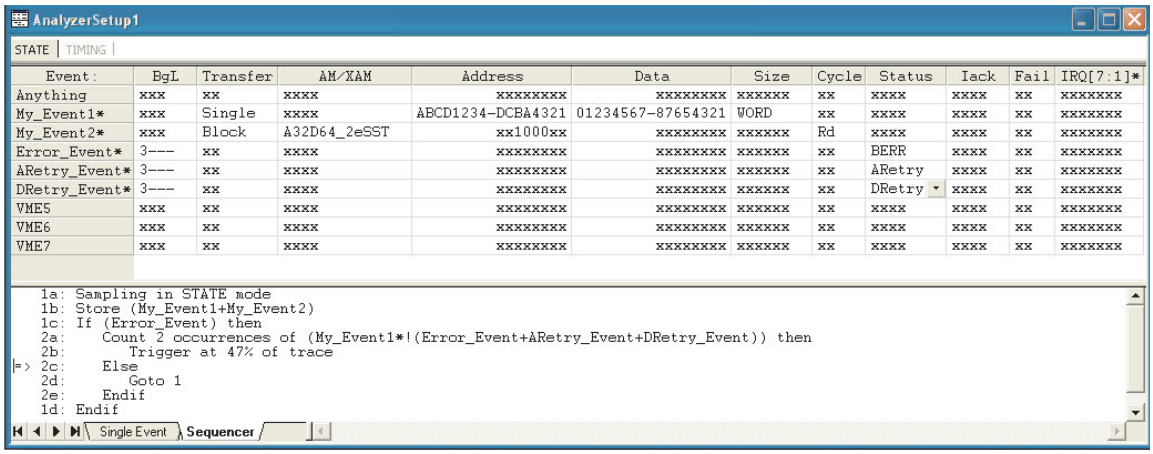


Figure 6: Advanced Trigger and Store Qualifier Example



State Analyzer

- State Analyzer and 133MHz Timing Analyze
- 2M Sample Trace Buffer @ 256-bits
- Extensive Trace Decoding with Mnemonics
- Time Tag and Latency Tag per sample
- Protocol Sensitive Sampling modes for optimum trace usage and readability
- Full Demultiplexing of Address, Data and other fields for maximum trigger and storage flexibility
- Multi-level Trace Viewer

The State Analyzer of the Vanguard VME captures and displays VMEbus activity in State or Timing modes with highly advanced (yet simple to use) triggering, filtering and counting capabilities. Unlike other logic analyzers, Curtiss-Wright's VME Bus Analyzers know the bus protocol of VMEbus, and derive the sampling clocks from the bus cycles at the right moments. This gives a complete trace of all kinds of activity, including arbitration, interrupts, block cycles, RMW etc.

Single Event Mode

In many cases a simple trigger like "If Event X then Trigger" is sufficient. For this purpose, the default "Single Event Mode" provides a trigger on the event pointed to in the Event Patterns window. When a more complex trigger is required, or a store or count qualifier is needed, the user may switch to the "Sequencer Mode".

Powerful Trigger and Store Qualifiers

To narrow in on the cycles of interest, Vanguard products are equipped with powerful triggers and store qualifiers, based on 8 full-width word recognizers and a flexible sequencer. Each of the word recognizers offers powerful operators like RANGE, NOT and BINARY for address and data fields etc., and the user may specify signal values as hex, binary or mnemonics like "Read", "Write", etc. This eliminates the need for the user to remember the actual signal values for the events and states on the bus.

Binary Details

Values for multi-bit fields like Address and Data are typically entered in hexadecimal format. But occasionally one may want to specify values of individual bits only, like setting bit 14 to 0 and/or bit 0 to 1, and so on. Called "Binary Details", this is another unique feature of Curtiss-Wright's Bus Analyzers. Pressing "(" when entering a number will switch to binary details mode.

Edge/Level Triggers

In order to make each event as powerful as possible, Curtiss-Wright's Vanguard product family has the ability to trigger on edges (rising, falling or both) as well as levels. This makes it easier for the user to specify a trigger, and hides unnecessary details from the user. As an example, triggering on the falling edge on the AS* signal would make sure the trigger is at the start of a transfer, whereas triggering on AS* being 0 could trigger in the middle of an ongoing transfer.

Figure 7: Binary Details

Event:	BgL	Transfer	AM/XAM	Address	Data	
Anything	xxx	xx	xxxx	xxxxxxxx	xxxxxxxx	xx
VME0	xxx	xx	xxxx	xxxxxxxx	xxxxxxxx	xx
VME1*	xxx	xx	xxxx	xxxxxxxx	xxxx(x0xx)xx(xxx1)	xx
VME2	xxx	xx	xxxx	xxxxxxxx	xxxxxxxx	xx
VME3	xxx	xx	xxxx	xxxxxxxx	xxxxxxxx	xx

16-Level Sequencer with 8 Events of 256-bits

The Vanguard provides an advanced 16-level Trigger Sequencer with powerful operators like IF, ELSIF, ELSE, STORE, COUNT, DELAY and GOTO. The sequencer is shown in a separate window on the main status screen, and may be used to define nested trigger conditions, define store qualifiers, count and delays statements. This sequencer is extremely powerful, since each event used contains 256-bits of information.

Figure 8: Sequencer in Graphical Mode

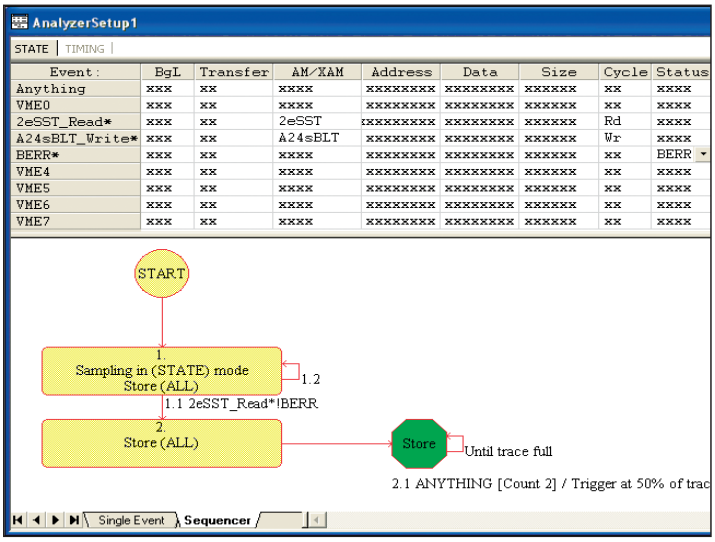
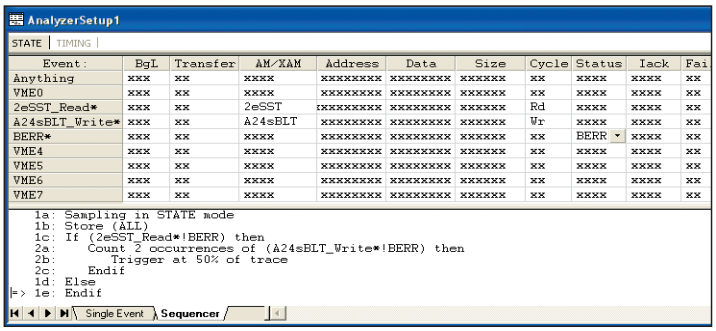


Figure 9: Sequencer in Text Mode



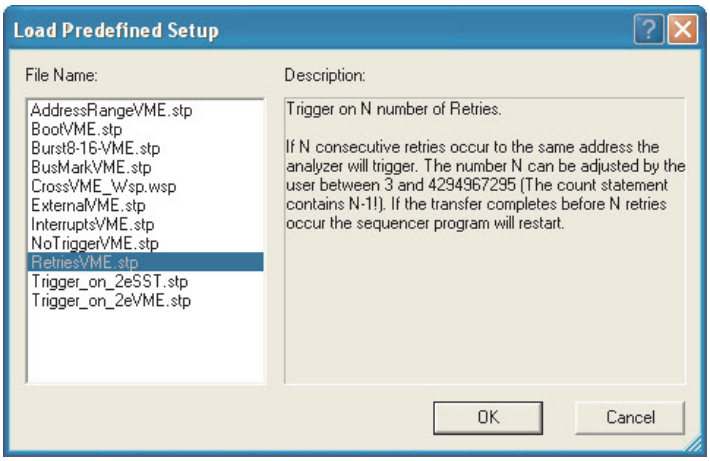
Adjustable Trigger Positions

For maximum flexibility, the trigger can be placed at any position in the trace buffer with a 1% resolution. This allows the user to utilize the 2 MSamples (64MB) of trace memory in the best possible way.

Example Setups

Example setups are provided to assist the novice user in defining trigger setups and to provide a "shortcut" to a number of typical trigger scenarios. BusView offers a function called "Predefined Setups". This function programs the event patterns and sequencer with the appropriate values and commands for the selected task (see dialog box below).

Figure 10: Predefined / Example Setups



Trigger Output

A Trigger Output signal is available on a pin header on the front panel. The LVTTL compatible signal has selectable polarity and mode, i.e. the signal may simply change logic level on trigger, or it may be selected to pulse when a trigger or a valid store condition occurs. The Trigger Output signal is useful for triggering external instruments such as high-speed oscilloscopes, counters, etc.

Multi-Level Trace Viewer

The powerful sampling modes of the Vanguard products, offer an innovative way of visualizing data captured in multiple views. This means the data can be viewed as summarized transactions when initially looking through the data, and then one can zoom in to look at individual clock cycles in a detailed waveform view when the point of interest is identified. This mode makes it possible for software and hardware engineers to view the data in their individual preferred views based on the same captured data.

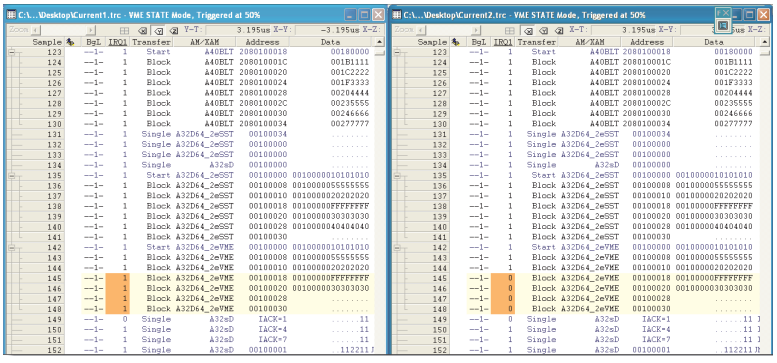
Search & Extract Trace Data

Powerful Search and Extract functions are provided for easy location of particular samples in the trace memory. After a trace is collected, any combination of signals can be searched for, extracted or hidden in the trace buffer.

Trace Compare

A powerful feature of BusView is the ability to compare the contents of the trace buffer with a trace stored on file on the host PC. This greatly simplifies error location by rapidly spotting differences between failing and functioning systems (see below). For example, a system works fine under some circumstances but not under others, or when one out of several presumably identical systems fails.

Figure 11: Trace Compare



Versatile Waveform Diagrams

When sampling in TIMING mode, the easy-to-read waveform diagrams provide powerful zooming, cursors and navigation tools. To ease the search for cycles of interest, one may use an "edge-to-edge" scroll mode on a selected signal, as well as explicit jumps to given line numbers or to cursors.

Save Trace to File

Captured trace data may easily be saved to a binary or ASCII file on a PC and then loaded back later. Partial traces may be loaded. Trace files may also be reviewed locally on the PC using the BusView for Windows software.

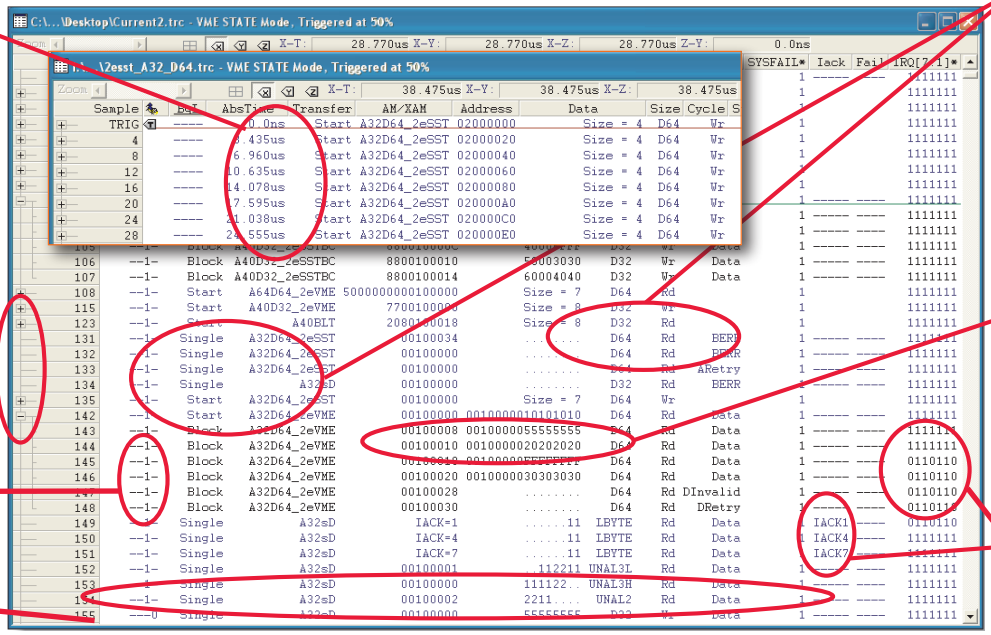
Figure 12: State Mode Sampling

Time Tag
Absolute time or relative time between samples as separate columns in trace.

Multi-level Trace Viewer
The ability to collapse and expand block transfers gives maximum overview without sacrificing detail.

Bus Grants
are latched during the arbitration to provide information about the current bus level in state analysis.

Decoding
All cycles are properly decoded and formated.



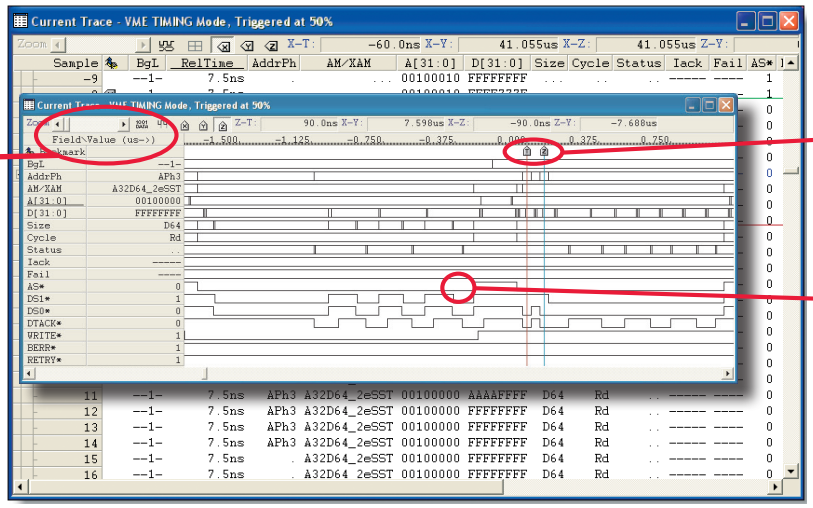
Mnemonics
are used for Transfer Size, Cycle Type, AM and XAM codes and Status to maximize readability.
The formatting supports all VMEbus transactions including 2eSST, VME64, IACK and RMW.

Demultiplexing
Full demultiplexing accross 64-bit Address and Data makes both trace readability and specifying a trigger easier.

Interrupts
The flow of Interrupt Request and Interrupt Acknowledge cycles can easily be read out from the trace listing.

Figure 13: Timing Mode Sampling

Zoom
Change from nano-second to second view instantly for maximum productivity.



Markers
Three markers can be positioned in the trace to allow timing measurements.

Edge Jumping
By highlighting a signal and then pressing the [tab] key, the view automatically jumps to the next edge on that signal.

Statistics

- Independent Real-time Statistics Engine
- 61 Real-time counters including 8 User-defined
- Pre-defined and User-defined statistics

Concurrent Statistics

The Vanguard's enhanced statistics engine offers concurrent Real-time measurements for Event Counting, Bus Utilization, Bus Transfer Rate, Block Length Distribution, Arbiter Latency and User Defined Statistics. The statistics engine uses hardware counters and pre-programmed word recognizers to generate the measurements displayed in each graph. The user may save the displayed statistics data to an ASCII file for post processing, analysis and display. It is also possible to play back statistics at a user selectable speed.

Bus Utilization

The Bus Utilization statistics function displays the percentage of time the bus is occupied, how much overhead a system has, and how the bus is being used at any given time. This statistics function is ideal for determining whether the bus has spare capacity to support additional I/O devices or processors.

Event Counting

The Event Counting function, provides a Real-time count of 8 user-defined events. This powerful function may be used to count the number of BERR cycles per second, to count the number of Write or Read cycles, or to investigate access patterns to the bus in multi-processor systems, etc.

Bus Transfer Rate

The Bus Transfer Rate function presents how much data is transferred over the bus, shown in MB/s. There are two different charts that display this information, one is per Bus Level and one is per Transfer Type (2eSST, 2eVME, MBLT, BLT or SCT). This statistics function is used to verify that system performance specifications have been fulfilled and to assist in system tuning.

Block Length Distribution

The Block Length Distribution function displays the distribution of block lengths broken into categories of single cycles, 2-7, 8-31, 32-127 and larger than 128 data phases. In addition Retry/BERR and RMW cycles are counted. Block Distribution statistics are very useful for measurements during performance enhancement and optimization.

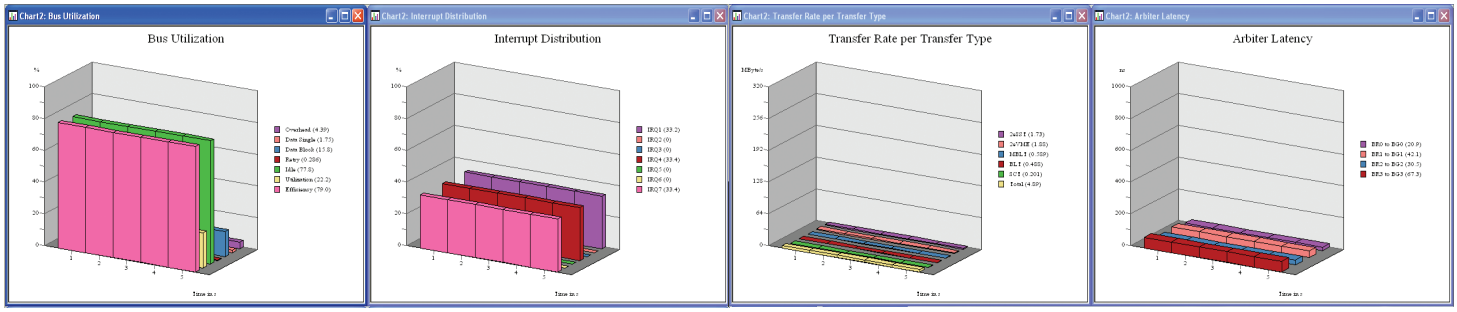
Interrupt & Interrupt Time Distribution

The Interrupt Distribution statistics function shows the distribution of IRQ1 through IRQ7 in the system, while the Interrupt Time Distribution shows the time it takes to service the various interrupt levels. Since many VME systems utilize interrupts extensively, this function is very useful in profiling a system and monitoring over time for abnormalities.

Arbiter Latency

The Arbiter Latency function shows the time between the assertion of BRx to the assertion of BGx.

Figure 14: Real-time Statistics Charts



Custom Statistics

This function allows the user to define up to 8 statistics functions using mathematical combinations of 61 (including 8 User-defined) Real-time counters available in the Vanguard VME product. This allows the user to implement a virtually unlimited number of statistics functions.

Exerciser

- VMEbus Master with 2 DMA engines
- Extensive Test Commands with walking ones/zeros, random patterns, etc.
- Built-in Script Recording and Playback
- Interrupt Generator and Handler
- VMEbus Slave memory with SW-controlled base address
- Full 2eSST protocol support
- Start Exerciser on Analyzer Trigger

The optional (-VE option) Exerciser available for the Vanguard VME is a powerful Master with a DMA engine, a Slave memory, a System Controller and an Interrupt Generator and Handler. The unit is very flexible and easy to use, and allows concurrent operation of all functions. A flexible script feature allows test scripts to be made and tasks to be automated.

The exerciser is controlled via dialog boxes through the user-interface, automated with the built-in script recording and playback capability with programmable delay and loop functions.

Simultaneous Exercising & Analysis

The Exerciser is a separate functional unit of the Vanguard board, which can start and run totally independently and concurrently with the analyzer. Similarly, the Slave interface is another separate functional unit with 8MB of memory. The Slave memory can be accessed by other VME devices at any time, with an address specified by the user.

Master with Powerful Data

The Bus Master has a DMA engine, allowing the user to test transactions to several slave devices concurrently. Normally, the DMA controller transfers data between the local memory and VME memory. However, a unique feature of the Vanguard Exerciser is the ability to transfer data with DMA from one VME device to another. Up to 8MB of data can be transferred per DMA command, with peak block transfer data rates of 320MB/s.

Figure 15: Exerciser Master Dialog Box

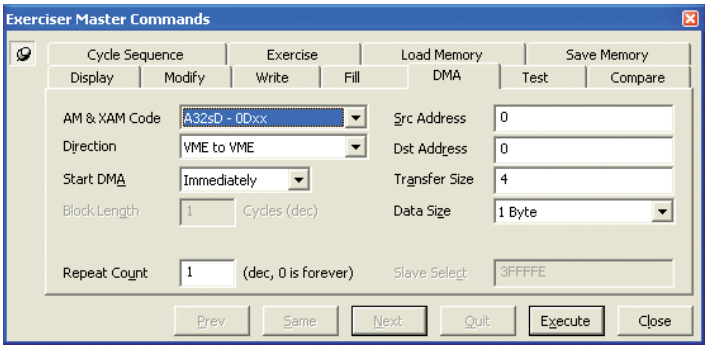
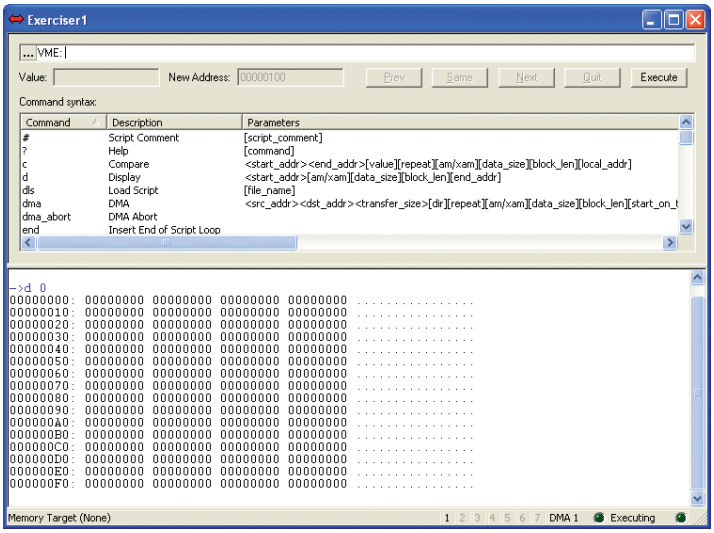


Figure 16: Exerciser Command-line Interface



Script Function Allows Automated Testing

A built-in script engine allows test scripts to be created with a convenient record and playback function. Scripts are recorded by manually running through the various commands of the exerciser. Several scripts can be stored and retrieved for later use. Each script consists of sequences of bus cycles of any kind, with varying sizes, cycle types, etc. The script playback function can be set to run single, multiple or infinite playbacks, while the analyzer part of the product may perform bus monitoring in the background. This makes the Vanguard ideal for running automated tests during design verification or production test of VME devices, adapters and motherboards.

Emulate a Board Under Design

In many cases a board intended for a specific system is not available. The Exerciser can emulate this card as a Slave or as a Master. This way the software design can progress without waiting for the hardware. The Exerciser also contains a slave interface that has its own address decoder for a user defined address window. This may respond to accesses from other modules.

Slave Memory

The module contains 8MB of Slave memory that can be located anywhere in the VME address map by a command in the user interface. Data can be written to and read from this memory as single cycles or as block transfer cycles for a peak bandwidth of 320MB/s.

Protocol Checker

- Automatically detects 60 VMEbus protocol errors including 2eSST protocol violations
- Trigger output to State Analyzer or External Output

The Vanguard VME Bus Analyzer features an optional protocol checker for the VMEbus (-VP option). This versatile feature automatically detects up to 60 VME errors, helping the user track down bus hardware errors without the need to understand the nature of the problem.

The protocol checker can run in the background when other analyzer functions of the Vanguard are active. As an example, the state analyzer, and the bus utilization statistics can all be active at the same time while the protocol checker runs in the background, screening the bus for errors. If the protocol checker is used as the trigger source for the analyzer(s), the state and timing analyzers will then provide a comprehensive picture of the bus activity around the point when an error was found. This helps the user to identify and correct the problem.

Figure 17: Protocol Checker Overview Window

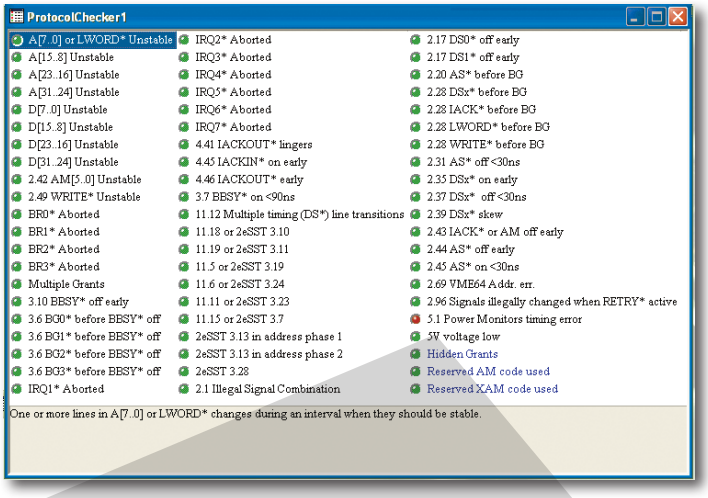


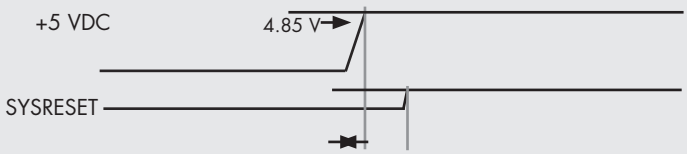
Figure 18: Help File Description of Violation

5.1 Power Monitors timing error

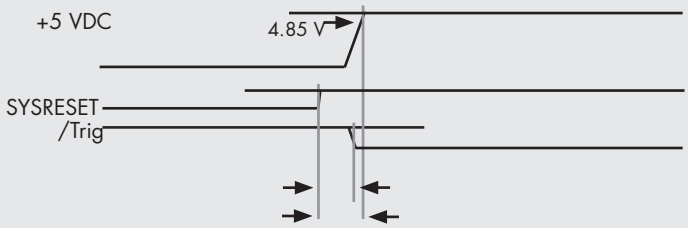
The "Rule 5.1 : SYSRESET* off < 4.85 V" violation is triggered when, during power up, the SYSRESET* signal goes away before the +5V power lines go above 4.85 volts. The VMEbus specification requires that SYSRESET* be held low until 200 ms after the +5V power goes to 4.875 volts. The Vanguard VME Protocol Checker is more lenient, requiring the +5V lines to reach at least 4.85 volts before SYSRESET* is released.

The following diagram illustrates normal operation as well as an error condition.

Normal Operation Example



Abnormal Operation Example



Miscellaneous

External Power Supply Provision

The Vanguard VME has provision for an external power supply (401-EPSU). This makes it possible to use the analyzer in systems with a marginal power supply.

Adding Optional Functionality

The Vanguard Product Range is based on a field programmable architecture that allows a single physical implementation to offer different functionalities. This means a user can purchase a Vanguard basic model (including the State Analyzer and Statistics), and later add the Protocol Checker by simply purchasing a new license key and entering that into the BusView software.

Additionally, the field programmable architecture allows Curtiss-Wright to offer new functionality not yet available to existing customers by way of a software update (BusView automatically checks for and downloads updates) and a license key.

Monitoring Temperatures and Voltages

When debugging systems both locally and remotely, experience has taught us that some hard-to-debug problems often are related to voltage drops and/or temperature variations. The Vanguard family of Bus Analyzers offers the ability both to monitor voltages and temperature, and to generate alarms if either voltages or temperatures fall outside a specified range.

The Vanguard Analyzer family is often used for complex monitoring and debugging applications. In order to track events such as temperature alarms, resets, protocol violations and triggers, a Status log window has been added.

Figure 19: Temperature and Voltage Monitoring

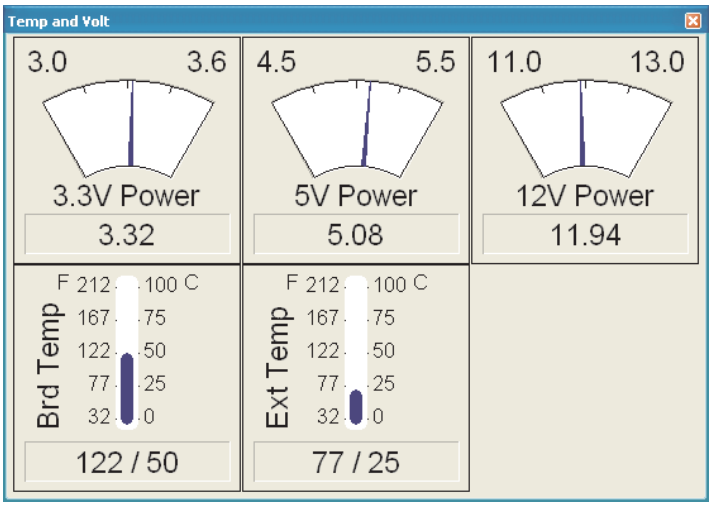




Table 2: Specifications

Analyzer		
Trace Memory	2M Samples x 256-bits (64MB total)	
Input Channels	101 bus signals, plus 16 ext. inputs on pin headers.	
Monitored Signals	A31-01, D31-00, DS1*, DS0*, AS*, LWORD*, DTACK*, BERR*, WRITE*, AM5-0, IRQ7-1*, IACK*, IACKIN/ OUT*, BBSY*, BR3-0*, BCLR*, RESP*, RETRY*, ACFAIL*, SYSFAIL*, SYSRES*, SYSCLK, XAM7-0, GA4-0, 2eSST_Trf_Rate3-0, SubUnit7-0, 2eSST_ Odd. BG3-0IN* SER_A, SER_B, RESP* also clocked separately, encoded and stored as Bus Level. RMW and Block w/VME64 internally generated. Cross trigger signals from the other functional units are also monitored.	
Trigger	8 word recognizers covering all 101 VMEbus signals and 16 Ext. inputs. True Range & NOT operator on Address/Data. Edge Triggering.	
Range	8 A64 address ranges, 8 D64 data ranges. Inside/Outside.	
Sequencer	16 levels with If, Else, Elsif, Goto, Count, Delay, Trigger, Store, Halt.	
Trigger Position	0-100%, 1% resolution AS* to Data Counter: 6-bits	
Cycle Counter	8-bits	
Occurrence / Delay Counters	3 x 32-bits	
Trigger Output	LVTTL level trigger output with programmable polarity, level or pulse. May pulse on each stored sample. Available on pin header in front panel.	
External Inputs	8 TTL level inputs on pin header 8 TTL level inputs on front pane	
Statistics		
Event counters	8 x 30-bits	
Real-Time Statistics Counters	53 x 30-bits counters	
Time Tag	Range	7.5ns-1172min
	Resolution	7.5ns
Exerciser (-VE Option)		
Master	Supports normal and block cycles on any BR level, selectable RWD, ROR, ROC or RNE release options.	
Slave	8MB SDRAM memory, with software controlled base address and window size	
Protocol Checker (-VP Option)		
VME Violations	60 Protocol Violations and 3 Protocol Warnings	

Table 3: Technical Specifications

General		
VMEbus	Up to 320MB/s (2eSST)	
Interfaces	-USB port, 12MB/s -Ethernet port 10/100MB/s	
Power Supply Requirements	+5VDC +/-5% from VME connector or from ext. power supply via front panel inlet.	
	Idle	1.5A (7.5W) VG-VME(-VP) 2.1A (10.5W) VG-VME(-VP)-VE
	Active	2.8A (14W) VG-VME(-VP) 4.0A VG-VME(-VP)-VE
Dimensions	160 x 233.4mm (6U)	
Compliant to	VMEbus Rev. D 1992 ANSI/VITA 1-1994 VME64-Standard ANSI/VITA 1.1-1997 VME64-Extensions ANSI/VITA 1.5-2003 2eSST	
Operating Temperature	0-50°C / 32-122°F	
Measurements	Temperature Probe	0-120°C/-32-248°F
	Voltage	3.3V, 5V, 12V



Table 4: Ordering Information

Ordering Information	
VG-VME	VME State Analyzer, 133MHz Timing Analyzer and Statistics Module. This board has NO P0 connector mounted. Includes BusView GUI.
VG-VMEP0	VME State Analyzer, 133MHz Timing Analyzer and Statistics Module. Includes P0 connector to allow Vanguard PMC module to access PCI/PCI-X on the P0 connector. Includes BusView GUI.
VG-VP	VMEbus Protocol Checker license key for Vanguard product line.
VG-VE	Exerciser Module for VG-VME product line.
Related Products	
VG-PMC	PMC State Analyzer and Statistics Module. (Single PMC for all functions) Includes BusView GUI. Can operate as P0 PCI/PCI-X Bus Analyzer for VG-VMEP0. (See separate datasheet)
VG-cPCI	cPCI-X & cPCI State Analyzer and Statistics Module for 5V and 3.3V systems. Includes cPCI carrier, SAM module and BusView GUI. (See separate datasheet)
VG-PCI	133MHz PCI-X & PCI State Analyzer and Statistics Module for 5V and 3.3V systems. Includes PCI-X carrier, SAM module and BusView GUI. (See separate datasheet)
VG-P	PCI-X & PCI Protocol Checker license key for Vanguard PCI/PMC/cPCI product line.
VG-E	100MHz PCI-X & PCI Exerciser and Compliance Checker license key for Vanguard PCI/PMC/cPCI product line.
VG-E2	100MHz PCI-X & PCI Enhanced Exerciser, Error Injector and Compliance Checker license key for Vanguard PCI/PMC/cPCI product line.

Individual boards and SAM modules may be purchased separately.

Packages are also available. Please consult Curtiss-Wright.

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwcdefense.com/sales

Email: defensesales@curtisswright.com

Technical Support

For technical support:

Website: www.cwcdefense.com/support

Email: support1@cwcembedded.com

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